



Intel® Wireless-AC 9560 (Jefferson Peak 2)

External Product Specification (EPS)

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Revision History

Revision	Description	Date
0.5	Initial release	September 2016
1.0	Corrected errors in CNVio trace numbers on M.2 2230 (pins 21 and 23 swapped) Changed interface name to CNVio on drawings and text Removed most of the SAR chapter (need to describe new DRS mechanism) Removed WiGig option Updated 3D drawings for 2230 and 1216 Updated drawing for MB layout examples (CNVi and Dual Design) Added KPIs: • Wi-Fi power consumption • Bluetooth® power consumption • Wi-Fi TPT targets • Wi-Fi sensitivity targets	April 2017
1.1	Fixed a typo in Table 5-7 (Wi-Fi performance, swapped 80 and 160MHz)	May 2017
1.2	Updated Wi-Fi Tx power per MCS as of QS milestone Updated Wi-Fi Rx sensitivity table 32KHz SUSCLK – defined as not used Removed 32KHz from drawings in Figure 1-1, Figure 2-2, and Figure 9-1 Updated DRS section Updated JfP2 1216SD drawings Updated Bluetooth® Tx power and sensitivity tables	July 2017
1.3	Updated Section 9.2, Boot sequence Updated Table 3-1, Hybrid Key E 2230-platform module pinout, to remove power levels on NC pins	September 2017
1.4	Added JfP 2230 Tx power regulatory limits Updated JfP 2230 power per MCS Removed statement about RGI not needing pull-ups in Section 2.2) Added missing PU in Table 9-2 Removed former Section 7.5; no HW SKU for SAR	October 2017
1.5	Added device weight	November 2017
1.6	Changed note (2) onTable 5-1, "Wi-Fi power consumption" Added comment on CTDp values in Section 6.1 Change Tx power back off to 0.5dB in Section 7 Removed DD (Delay Diversity) and BFER from regulatory tables Added CLK 38.4MHz characteristics table in Section 9.1.9.3 Updated Section 7.5 with SAR considerations	November 2017



Revision	Description	Date
1.7	Updated JfP 2230 power per MCS (default values) Updated JfP 1216 power per MCS Added JfP2 1216 WiFi Rx Sensitivity Added JfP2 1216 regulatory tables Added a comment about SRD Tx power limits Updated SAR minimum distance to be 15mm instead of 18mm	January 2017
1.8	Updated CNVi power on timing. T4-T3>0 Added 20MHz regulatory tables for 1216 in Sections 7.4.5, 7.4.6, 7.4.7	March 2018
1.9	Updated Table 9-4, "38.4MHz clock signal characteristics"	April 2018
2.0	Updated characteristic impedance to 85 ohm, added GPIO signal mapping Updated SKUs in Table 1-2 with 80MHz SKU and fixed typo Fixed typo in W_DISABLE1# description in Table 3-1 and Table 3-2 Clarified that the W_DISABLE2# pull-up is tied to internal 1.8V level in Table 3-1 and Table 3-2. Updated Table 3-3 with BRI/RGI rise and fall time Added notes about the actual shield size compared to the drawing in Figure 4-1 and Figure 4-3 Added a note about 1216 PCB height in Figure 4-3 Updated antenna connector Table 4-2 and Table 4-3 with label and M.2 designations Added new Table 7-1 with active/passive scan values Added note about Ukraine EIRP limits in Table 7-2 Fixed MIMO 2 column for JfP2 20MHz Tx power in Table 7-5 Removed duplication of 1216 SD pinout drawing (previous Figure 9-3)	August 2018
2.1	Updated Bluetooth® Tx power and sensitivity data in Table 5-8 and Table 5-9	September 2018
2.2	Added that MU-MIMO is supported	September 2018
2.3	Updated pinout information in Table 3-1 (added M.2 standard pinout names for 2230) and Table 3-2 (added platform naming and I/O direction for 1216) Removed redundant TBD Updated notes in Table 5-8 and Table 5-9: Bluetooth® 1216 numbers refer to LTE and non-LTE modules Added Section 11, Intel® PROSet/Wireless Software for Bluetooth® Technology v20.0	October 2018
2.4	Fixed incorrect block diagram in Figure 1-1	January 2, 2019
2.5	Added electrical specifications for W_DISABLE1# and W_DISABLE2# pins in Table 9-5 and Table 9-6 Updated Section 11, Intel® PROSet/Wireless Software for Bluetooth® Technology v20.0	February 12, 2019
2.6	Added a reference to TA #574558 for ESD risk reduction in Section 9.1.9.3	March 1, 2019



Revision	Description	Date
2.7	Changed LTE module name typo to 7360 Updated JfP2 1216 weight in Table 4-1 Fixed typo in de-coupling description in Section 9.1.11: 3.3 V pins updated to 72 and 74 Fixed CNVio clock rate typo in Section 9.1.9.1	June 20, 2019
2.71	Added accuracy for Wi-Fi Rx KPIs (+/- 0.5 dB) Updated scan policies per sub-band and country setting in Table 7-1	July 18, 2019
2.72	Updates in compliance with the Bluetooth® 5.1 Core Specification. Updated Section 11.2.3 to remove the periodic advertising feature, which is no longer supported.	April 24, 2020
2.8	Updated Table 5-3 and Table 5-4 based on latest fixes made in software version 22.0	September 24, 2020
2.81	Added a note about End of Life of the Jefferson Peak 2 LTE Coex SKU	March 25, 2021



Abbreviations

Term	Description
CNVi	Integrated connectivity solution
CRF	Companion RF chip/module of the CNVi
SoC	System on chip
PCH	Platform control hub
Pulsar	The integrated IP part of the CNVi
JfP	Jefferson Peak companion RF chip/module
LTE	Long-term evolution (a mobile phone standard)
RGI	Radio generic interface, between JfP and Pulsar
BRI	Bluetooth® radio interface, between JfP and Pulsar
Wi-Fi	Wireless LAN
OTP	One-Time Programmable non-volatile memory
LDO	Low-Dropout Regulator
I/O	Input/Output
GPIO	General-Purpose Input/Output
RTC	Real-Time Clock
DC	Direct Current
CNVio	High-speed data interface for CNVi
DPHY	Differential PHY (high-speed serial bus)
MIPI	Mobile Industry Processor Interface
RF	Radio Frequency
IOSF	Intel On-chip System Fabric
Coex	Coexistence
UART	Universal Asynchronous Serial Bus
I2C	Inter-Integrated Circuit bus
ISH	Integrated sensor hub
CLINK	Control Link
AMT	Intel® Active Management Technology
USB	Universal Serial Bus





1 Introduction

The Intel® Integrated Connectivity Wireless-AC 9560 (code name Jefferson Peak or JfP) is an M.2 connectivity RF companion module for notebooks, tablets, and PCs. When combined with the Intel SoC that supports Connectivity Integration (CNVi), it supports the following radio technologies:

- 802.11abgn + acR2 MIMO 2x2 + MU-MIMO
- Bluetooth® 5.1

The product is a highly-integrated solution; the silicon design is based on the 28 nm process, and has a new architecture that splits the Wi-Fi and Bluetooth® radio blocks into an integrated MAC block (residing in the Intel SoC) and the PHY/RF block (residing in the RF companion module). This solution provides higher level of integration with Intel platforms, and a set of advanced capabilities. The Jefferson Peak family includes two products:

- JfP2 – A module with Wi-Fi-2x2 radio (2 Wi-Fi chains) and Bluetooth®
- JfP1 – A module with Wi-Fi 1x1 radio (single chain) and Bluetooth®. For further details about the 1x1 version, please refer to the JfP1 EPS.

The product is designed to be part of the Intel® Cannon Lake and Gemini lake platforms, supporting Microsoft* Windows* Threshold version as well as the Google* Chrome OS* and Linux*.

1.1 Key features

Table 1-1 Key features (when connected to the MAC part residing in the SoC)

Feature	Jefferson Peak
Platform	Cannon Lake Y, U, H, DT Gemini Lake Connected standby and traditional platform types
Form Factor and SKUs	• M.2 2230 • M.2 1216 soldered-down module
Wi-Fi	High performance low power dual band 802.11acR2 2x2 + MU-MIMO
Bluetooth®	Bluetooth® 5.1
Host Interfaces	Wi-Fi: PCI based (Internal to the SoC) Bluetooth®: USB based (Internal to the SoC), optional UART/I2S (Internal to the SoC) Intel® AMT: CLINK (Internal to the SoC)
Interfaces to the SoC	Wi-Fi: CNVio (Intel proprietary bus inspired by the DPHY low power interface) Bluetooth®: BRI asynchronous serial bus (Intel proprietary) Control: RGI asynchronous serial bus (Intel proprietary) Clock: Single-ended, 38.4MHz (These interfaces connect the RF companion module to the MAC part which is integrated into the Intel SoC)
Wi-Fi Alliance certifications	802.11a/b/g/n/ac , WPA/2 Personal and Enterprise, WPS2, 802.11w, WMM, WMM-PS, WFD, Miracast, Passpoint R2, Voice Personal
Wi-Fi-Bluetooth® Coex	MIMO Tx/Tx and Rx/Rx Concurrency
LTE Coex	Real-Time and Non Real-Time, LTE filter (not supported by all SKUs, see SKU description below)

Introduction

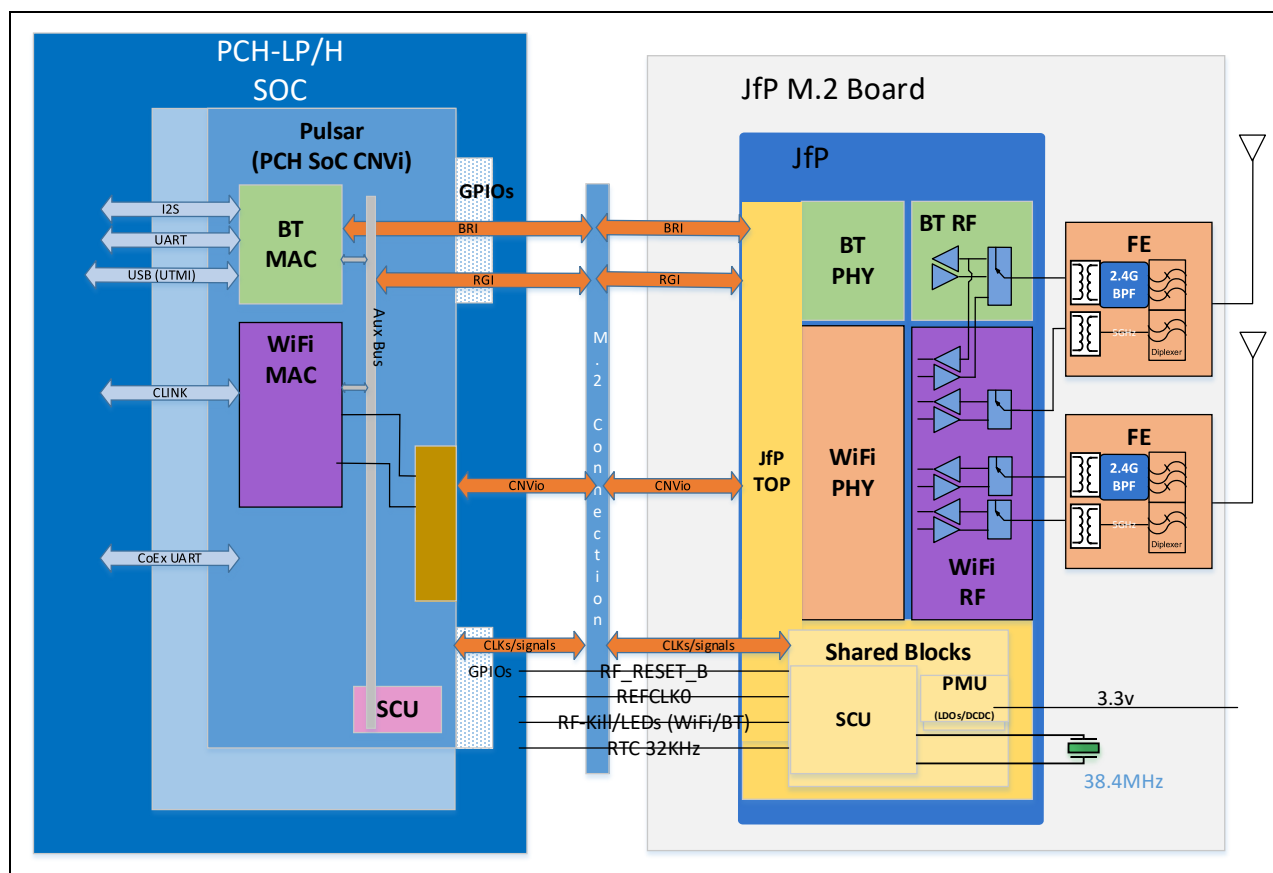
Feature	Jefferson Peak
Performance	Tx Burst, TCP packet reordering, MSIx for reduced multi-core CPU load
vPro	Intel® AMT 11.0
Miracast	
Smart SKU	Dynamic Regulatory SKU enabling automatic channel map and output power changes depending on the regulations of the country where it is operating
CNVi/Discrete auto-detect	Supports auto-detection by the SoC and by BIOS
Operating System	Windows 8.1*, Windows 10*, Linux*, Chrome OS*

NOTES:

1. This module must be used with an Intel SoC which supports Connectivity Integration (CNVi).
2. Real-time and Non Real-time LTE coexistence supported with Intel LTE 7360.

Figure 1–1 depicts the Jefferson Peak architecture.

Figure 1–1 Jefferson Peak module block diagram



Note: 2.4GHz band pass filters (BAW) for LTE coex will be supported on specific HW SKUs.



1.2 Jefferson Peak module SKUs

The Jefferson Peak module supports the HW SKUs listed in Table 1-2.

Note: The Jefferson Peak 2 LTE Coex SKU is at its EOL, starting from WW07'21. There is no impact to the other Jefferson Peak 2 SKUs. For additional details, please refer to document #635096.

Table 1-2 Jefferson Peak module SKUs

SKU Name	Form Factor	vPro Options	LTE Coex Options
JfP1 2230	2230 Hybrid Key E S3	Non vPRO	No LTE coex
JfP1-SD	1216 S3	Non vPRO	No LTE coex
JfP2 2230	2230 Hybrid Key E S3	vPRO/Non vPRO	Without LTE coex
JfP2-SD	1216 S3	vPRO/Non vPRO	With LTE coex (EOL)/ Without LTE coex
JfP2 80MHz 2230	2230 Hybrid Key E S3	Non vPRO	No LTE coex
JfP2 80MHz SD	1216 S3	Non vPRO	No LTE coex
JfP2 No regulatory	2230 Hybrid Key E S3	Non vPRO	No LTE coex



2 Product Architecture

2.1 Integrated Connectivity concept

2.1.1 MAC-PHY split

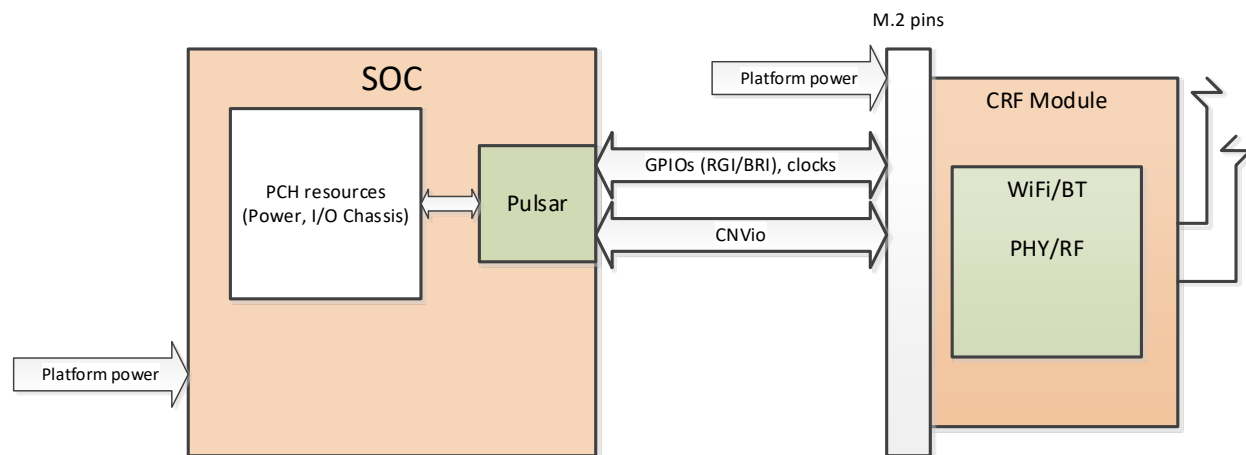
Integrated Connectivity (CNVi) is a new architecture for wireless connectivity devices. The concept of CNVi is to move a large part of the functional content of the connectivity chip from the radio chip into the Intel SoC. As a result, a large portion of the chip logic and memory resources is moved out of the radio chip while reducing the platform's bill of material (BOM) size and cost.

In the CNVi architecture, the MAC components of the Wi-Fi and Bluetooth® cores, including processors, logic, and memory, are relocated from the radio chip into the SoC chip. Signal processing, analog and RF functions stay in the radio chip, which is called a Companion RF (CRF) chip or module in CNVi terminology.

The part of the connectivity chip that is ported into the SoC is called Pulsar. Pulsar interfaces with the rest of the SoC functions through SoC-internal interfaces and busses, and does not require any external host interfaces at the platform level. On the other hand, interfacing Pulsar with the CRF module does require platform signals to be routed between the SoC and the CRF module. The CNVi architecture and the MAC-PHY split is shown in Figure 2-1.

The integrated connectivity architecture places the MAC component of the Wi-Fi and Bluetooth® cores inside the SoC. As a result, the host interfaces of Wi-Fi and Bluetooth® are no longer part of the M.2 module, which is a Companion RF module. These host interfaces reside in the SoC and are not exposed to the platform.

Figure 2-1 CNVi architecture



2.1.2 SoC and Companion RF compatibility

In order to use the integrated connectivity architecture, the platform needs to include both an SoC and a connectivity device which supports CNVi. This means that the SoC needs to have the Pulsar block integrated, and a Companion RF module should be used in the design. The Jefferson Peak Companion RF module can support the following Intel SoC devices, which include Pulsar:

- Cannon Lake PCH-LP
- Cannon Lake PCH-H
- Gemini Lake

2.1.3 Swappable Companion RF/Discrete

Companion RF (CRF) M.2 modules are swappable with discrete connectivity M.2 modules.

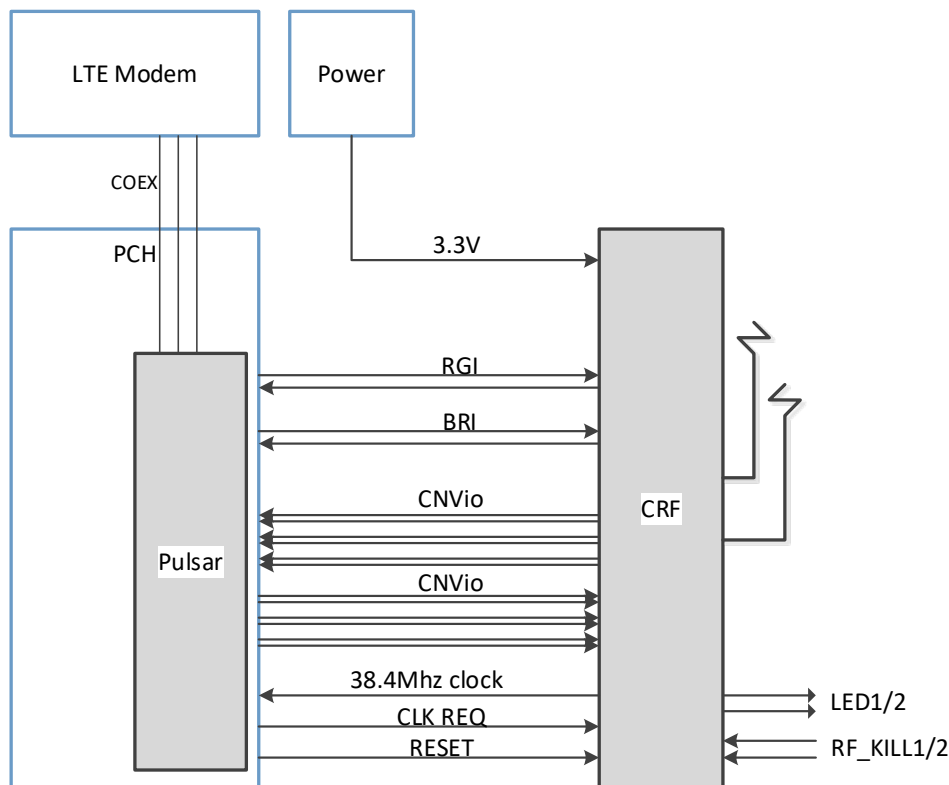
The meaning of swappable in this context is that the design of the M.2 socket on the platform can allow using the same M.2 socket for both CNVi and discrete connectivity without the need to change the hardware configuration. When designing the platform to support swappable CRF/discrete, a CRF module can be changed to a discrete module, and vice versa, by simply removing one M.2 card type from the socket and swapping it with a new card type. Note that M.2 does not support hot-swapping and therefore the platform power should be turned off before doing this operation. The swappable concept is also applicable to 1216 soldered-down versions of the CRF, which also allows the same PCB design to have a single footprint supporting either a 1216-SD JfP CRF or a standard M.2 1216 discrete (not integrated) module. Obviously, in the soldered-down case, swapping modules will require disassembling the soldered module from the board.

In order to design the platform to support both discrete and CNVi, and have the swappable feature, the platform needs to be designed properly. The specific guidelines for this type of design will be shown in the platform design guidelines section of this document.

2.2 Jefferson Peak interfaces

The Jefferson Peak interfaces are illustrated in Figure 2–2.

Figure 2–2 Jefferson Peak interfaces





Product Architecture

The Jefferson Peak M.2 module interfaces the platform and the SoC through a proprietary interface for CNVi. This interface connects between the JfP module and the SoC and between the JfP module and the platform. A high-level description of the interface is shown in Figure 2–2.

Power supply

The Jefferson peak module is powered by a 3.3V supply connected to the dedicated power pins on the M.2 module connector. Proper decoupling capacitors are required to be placed close to the module/socket pins. See more details in Section 3.

32KHz clock

The Jefferson Peak 2 module uses an internal slow clock for low power states and does not need to get the 32Khz slow clock from the platform. The recommendation is to leave this pin not-connected.

BRI/RGI

These are two serial asynchronous busses used for Bluetooth® traffic (BRI) and for control data (RGI). Each bus has one signal per direction. The BRI and RGI busses do not require any clock to be sent with the data lines as the clock at the receiving end of the bus is extracted from the data itself. The BRI and RGI toggle at 76.4Mbouds each (full duplex). The signals are standard 1.8V logic level.

CNVio

The CNVio signals connect the JfP module and the SoC. They are used as the main data bus for Wi-Fi, to transfer data between the Pulsar and the RF companion chip. The CNVio signals are physically similar to the MIPI DPHY standard, but have a different (and Intel-proprietary) protocol.

The CNVio bus has two data lanes and one clock for each direction. Both data and clock signals are differential, 85-Ohm signals. The total number of signals for the interface is 12 (6 pairs, 3 per direction). These signals should be routed as differential, controlled impedance traces. Due to the sensitivity of the CNVio bus to signal impairments, RF layout techniques and good length matching shall be used. Section 9.1.9.1 contains specific design guidelines for the CNVio routing.

Reference clock (38.4MHz)

This is the main clock used for both Pulsar (the MAC part which is inside the SoC) and Jefferson Peak. The clock is driven by the JfP output clock buffer at voltage levels of 1V (pk-pk). This clock shall be routed from JfP to the SoC with special care to minimize clock jitter. Section 9.1.9.3 contains specific design guidelines for the reference clock routing.

Reset and Clock Request

The Reset and Clock Request signals are automatically driven by the SoC to control the operation of the Companion RF and minimize system power consumption. The SoC uses the Reset only at initial power up. The Clock Request signal is used to change the Jefferson Peak power modes between high-power clock and low-power clock (per the system power states).

LEDs

Jefferson Peak M.2 module supports driving two LEDs to indicate wireless activity. These pins have open-drain buffers which sinks current (logical zero) when the LED is turned on.

RF-KILL

Jefferson Peak M.2 module SKUs support wireless disable (RF-KILL) command through the two RF-KILL pins for turning off Wi-Fi and Bluetooth® respectively. These pins can be connected to a platform switch or SoC GPIOs.





3 Electrical Specifications

This section provides information about the electrical specifications of the Jefferson Peak module. The specifications cover the module hardware interface signals.

3.1 2230 and 1216 form factor pinouts

There are two pinout lists, one for the platform side, and one for the module side. Note that some signals are crossed (such as UART Rx on platform side is connected to TX on the module side).

Note: The 2230 module pinout is based on the Hybrid Key E scheme. The Hybrid Key E is an Intel-proprietary scheme, which is based on the mechanical and electrical specifications of the PCIe* M.2 Electromechanical Spec, modified by changes to the pinout in order to support Intel's Integrated Connectivity (CNVi).

Table 3-1 Hybrid Key E 2230-platform module pinout

Pin #	Pin Name Platform Pinout	Pin Name Module Pinout	M.2 Standard module point of view	Direction w/respect to JfP Module	JfP Voltage on Module Side	Connection on Platform/Usage
1	GND	GND	GND			
2	3.3 V	3.3 V	3.3 V		3.3 V	3.3 V Supply
3	USB_D+	NC	USB_D+			Not used by Jefferson Peak Shall be connected to USB for supporting discrete module
4	3.3 V	3.3 V	3.3 V		3.3 V	3.3 V Supply
5	USB_D-	NC	USB_D-			Not used by Jefferson Peak Shall be connected to USB for supporting discrete module
6	LED1#	LED1#	LED1#	O	OD	Wi-Fi LED
7	GND	GND	GND			
8	PCM_CLK/I2S SCK	NC	PCM_CLK/I2S SCK			Not used by Jefferson Peak Optional PCM interface for supporting discrete module
9	WGR_D1N	WGR_D1N	SDIO CLK	O	CNVio PHY	CNVio bus RX lane 1
10	PCM_SYNC/I2S WS/RF_RESET_B	RF_RESET_B	PCM_SYN C/I2S_WS	I	1.8 V	Jefferson peak RF (active low) Optional PCM interface for supporting discrete module
11	WGR_D1P	WGR_D1P	SDIO CMD	O	CNVio PHY	CNVio bus RX lane 1
12	PCM_IN/I2S SD_IN	NC	PCM_IN/I2S_SD_OUT			Not used by Jefferson Peak Optional PCM interface for supporting discrete module
13	GND	GND	SDIO DATA0			
14	PCM_OUT/I2S SD_OUT/CLKREQ0	CLKREQ0	PCM_OUT/I2S_SD_IN	I	1.8 V	Clock request for the 38.4MHz clock (CNVi reference clock) Optional PCM interface for supporting discrete module



Electrical Specifications

Pin #	Pin Name Platform Pinout	Pin Name Module Pinout	M.2 Standard module point of view	Direction w/respect to JfP Module	JfP Voltage on Module Side	Connection on Platform/Usage
15	WGR_D0N	WGR_D0N	SDIO DATA1	O	CNVio PHY	CNVio bus RX lane 0
16	LED2#	LED2#	LED2#	O	OD	Bluetooth® LED
17	WGR_D0P	WGR_D0P	SDIO DATA2	O	CNVio PHY	CNVio bus RX lane 0
18	GND	LNA_EN	GND			This a special purpose test pin of the JfP module. Should be connected to Ground on the platform.
19	GND	GND	SDIO DATA3			
20	UART WAKE#	NC	UART WAKE#			Not used by Jefferson Peak Optional PCM interface for supporting discrete module
21	WGR_CLKN	WGR_CLKN	SDIO WAKE#	O	CNVio PHY	CNVio bus RX clock
22	UART RXD/BRI_RSP	BRI_RSP	UART TXD	O	1.8 V	BRI bus RX Optional PCM interface for supporting discrete module
23	WGR_CLKP	WGR_CLKP	SDIO RESET#	O	CNVio PHY	CNVio bus RX clock
24	Connector Key	Module Key	Module Key			
25	Connector Key	Module Key	Module Key			
26	Connector Key	Module Key	Module Key			
27	Connector Key	Module Key	Module Key			
28	Connector Key	Module Key	Module Key			
29	Connector Key	Module Key	Module Key			
30	Connector Key	Module Key	Module Key			
31	Connector Key	Module Key	Module Key			
32	UART TXD/RGI_DT	RGI_DT	UART RXD	I	1.8 V	BRI bus TX Optional PCM interface for supporting discrete module
33	GND	GND	GND			
34	UART CTS/RGI_RSP	RGI_RSP	UART_RTS	O	1.8 V	RGI bus RX Optional PCM interface for supporting discrete module



Electrical Specifications

Pin #	Pin Name Platform Pinout	Pin Name Module Pinout	M.2 Standard module point of view	Direction w/respect to JfP Module	JfP Voltage on Module Side	Connection on Platform/Usage
35	PETp0	NC	PERp0			Not used by Jefferson Peak Shall be connected to PCIe* for supporting discrete module
36	UART RTS/BRI_DT	BRI_DT	UART_CTS	I	1.8 V	BRI bus TX
37	PETn0	NC	PERn0			Not used by Jefferson Peak Shall be connected to PCIe* for supporting discrete module
38	CLINK RESET	NC	VENDOR DEFINED			Not used by Jefferson Peak Optional CLINK interface for supporting discrete module
39	GND	GND	GND			
40	CLINK DATA	NC	VENDOR DEFINED			Not used by Jefferson Peak Optional CLINK interface for supporting discrete module
41	PERp0	NC	PRTp0			Not used by Jefferson Peak Shall be connected to PCIe* for supporting discrete module
42	CLINK CLK	NC	VENDOR DEFINED			Not used by Jefferson Peak Optional CLINK interface for supporting discrete module
43	PERn0	NC	PETn0			Not used by Jefferson Peak Shall be connected to PCIe* for supporting discrete module
44	COEX3 (I/O)	NC	COEX3 (I/O)			Not used by Jefferson Peak Optional Coex interface with LTE modem for supporting discrete module See more details in Section 9.1.9.4
45	GND	GND	GND			
46	COEX2		COEX2			Not used by Jefferson Peak Optional Coex interface with LTE modem for supporting discrete module See more details in Section 9.1.9.4
47	REFCLKP0	NC	REFCLKP0			Not used by Jefferson Peak Shall be connected to PCIe* for supporting discrete module
48	COEX1	NC	COEX1			Not used by Jefferson Peak Optional Coex interface with LTE modem when used with Discrete See more details in Section 9.1.9.4



Electrical Specifications

Pin #	Pin Name Platform Pinout	Pin Name Module Pinout	M.2 Standard module point of view	Direction w/respect to JfP Module	JfP Voltage on Module Side	Connection on Platform/Usage
49	REFCLKN0	NC	REFCLKN0			Not used by Jefferson Peak Shall be connected to PCIe* for supporting discrete module
50	SUSCLK (32 kHz)	C_P32K (32 kHz)	SUSCLK (32 kHz)	I	3.3 V	Not used by Jefferson Peak
51	GND	GND	GND			
52	PERST0#	NC	PERST0#			Not used by Jefferson Peak Shall be connected to PCIe* for supporting discrete module
53	CLKREQ0#	NC	CLKREQ0 #			PCIe* clock request. Not used by Jefferson Peak. Shall be connected to PCIe* for supporting discrete module.
54	W_DISABLE2#	W_DISABLE2#	W_DISABLE2#	I	3.3 V	JfP also supports 1.8 V electrical levels on this signal. This signal has an internal pull-up tied to 1.8V.
55	PEWAKE0#	NC	PEWAKE0 #			Not used by Jefferson Peak Shall be connected to PCIe* for supporting discrete module
56	W_DISABLE1#	W_DISABLE1#	W_DISABLE1#	I	3.3 V	JfP also supports 1.8 V electrical levels on this signal. This signal has an internal pull-up tied to 1.8V.
57	GND	GND	GND			
58	I2C DATA/ A4WP_I2C_DATA	NC	I2C DATA			Not used by Jefferson Peak
59	WT_D1N	WT_D1N	PERp1	I	CNVio PHY	CNVio bus TX lane 1
60	I2C CLK/ A4WP_I2C_CLK	NC	I2C CLK			Not used by Jefferson Peak
61	WT_D1P	WT_D1P	PERn1	I	CNVio PHY	CNVio bus TX lane 1
62	ALERT#/ A4WP_IRQ#	NC	ALERT#			Not used by Jefferson Peak
63	GND	GND	GND			
64	REFCLK0	REFCLK0	REFCLK0	O	1 V	38.4MHz clock from the JfP Module to the SoC
65	WT_D0N	WT_D0N	PETp1	I	CNVio PHY	CNVio bus TX lane 0
66	PERST1#	NC	PERST#1			Not used by Jefferson Peak
67	WT_D0P	WT_D0P	PETn1	I	CNVio PHY	CNVio bus TX lane 0
68	CLKREQ1#	NC	CLKREQ1 #			Not used by Jefferson Peak



Electrical Specifications

Pin #	Pin Name Platform Pinout	Pin Name Module Pinout	M.2 Standard module point of view	Direction w/ respect to JfP Module	JfP Voltage on Module Side	Connection on Platform/Usage
69	GND	GND	GND			
70	UIM_POWER_SRC/GPIO1/PEWAKE1#	NA	UIM_POWER_SRC/GPIO1/PEWAKE1#			Not used by Jefferson Peak
71	WT_CLKN	WT_CLKN	REFCLKP1	I	CNVio PHY	CNVio bus TX clock
72	3.3 V	3.3 V	3.3 V			3.3 V Supply
73	WT_CLKP	WT_CLKP	REFCLKN1	I	CNVio PHY	CNVio bus TX clock
74	3.3 V	3.3 V	3.3 V			3.3 V Supply
75	GND	GND	GND			

Table 3-2 1216-platform module pinout

Pin #	Pin Name platform pinout	Pin Name module pinout	Direction w/ respect to JfP Module	Function when CNVi is used	Function when Standard (discrete) M.2 is used	Comments
1	UIM_POWER_SRC/GPIO1	N/A		Not used	UIM_POWER_SRC/GPIO1	
2	UIM_POWER_SNK	N/A		Not used	UIM_POWER_SNK	
3	UIM_SWP	N/A		Not used	UIM_SWP	
4	3.3V	3.3V		3.3V	3.3V	
5	3.3V	3.3V		3.3V	3.3V	
6	GND	GND		GND	GND	
7	RESERVED	RESERVED		Not used	RESERVED	
8	ALERT#	N/C		Not used	ALERT#	
9	I2C_CLK	N/C		Not used	I2C_CLK	
10	I2C_DATA	N/C		Not used	I2C_DATA	
11	COEX_TXD	N/C		Not used	COEX_TXD	Not used by Jefferson Peak Optional Coex interface with LTE modem for supporting discrete module See more details in Section 9.1.9.4



Electrical Specifications

Pin #	Pin Name platform pinout	Pin Name module pinout	Direction w/ respect to JfP Module	Function when CNVi is used	Function when Standard (discrete) M.2 is used	Comments
12	COEX_RXD	N/C		Not used	COEX_RXD	Not used by Jefferson Peak Optional Coex interface with LTE modem for supporting discrete module See more details in Section 9.1.9.4
13	COEX3	N/C		Not used	COEX3	
14	SYSCLK/GNSS0	N/C		Not used	SYSCLK/GNSS0	
15	TX_BLANKING/GNSS1	N/C		Not used	TX_BLANKING/GNSS1	
16	RESERVED	RESERVED		Not used	RESERVED	
17	GND	GND		GND	GND	
18	RESERVED	RESERVED		Not used	Not used	
19	RESERVED	RESERVED		Not used	Not used	
20	GND	GND		GND	GND	
21	RESERVED	RESERVED		Not used	Not used	
22	RESERVED	RESERVED		Not used	Not used	
23	GND	GND		GND	GND	
24	RESERVED	RESERVED		Not used	Not used	
25	RESERVED	RESERVED		Not used	Not used	
26	GND	GND		GND	GND	
27	SUSCLK(32kHz)(3.3V)	N/C		32KHz clock (3.3V)	SUSCLK(32kHz) (3.3V)	Not used by Jefferson Peak
28	W_DISABLE1#	W_DISABLE1#	I	W_DISABLE1#	W_DISABLE1#	This signal has an internal pull-up tied to 1.8V
29	PEWAKE#	N/C		Not used	PEWAKE#	
30	CLKREQ#	N/C		Not used	CLKREQ#	
31	PERST#	N/C		Not used	PERST#	
32	GND	GND		GND	GND	
33	REFCLKN0	N/C		Not used	REFCLKN0	
34	REFCLKP0	N/C		Not used	REFCLKP0	
35	GND	GND		GND	GND	
36	PERn0	N/C		Not used	PERn0	



Electrical Specifications

Pin #	Pin Name platform pinout	Pin Name module pinout	Direction w/ respect to JfP Module	Function when CNVi is used	Function when Standard (discrete) M.2 is used	Comments
37	PERp0	N/C		Not used	PERp0	
38	GND	GND		GND	GND	
39	PETn0	N/C		Not used	PETn0	
40	PETp0	N/C		Not used	PETp0	
41	GND	GND		GND	GND	
42	CLink_CLK	N/C		Not used	CLink_CLK	
43	CLink_DATA	N/C		Not used	CLink_DATA	
44	CLink_RESET	N/C		Not used	CLink_RESET	
45	SDIO_RESET#	N/C		Not used	Not used	SDIO is not supported
46	SDIO_WAKE#	N/C		Not used	Not used	SDIO is not supported
47	SDIO_DATA3	N/C		Not used	Not used	SDIO is not supported
48	SDIO_DATA2	N/C		Not used	Not used	SDIO is not supported
49	SDIO_DATA1	N/C		Not used	Not used	SDIO is not supported
50	SDIO_DATA0	N/C		Not used	Not used	SDIO is not supported
51	SDIO_CMD	N/C		Not used	Not used	SDIO is not supported
52	SDIO_CLK	N/C		Not used	Not used	SDIO is not supported
53	UART_WAKE# (3.3V)	N/C		Not used	UART_WAKE# (3.3V)	
54	LPSS_UART_RTS/br i_dt	N/C		Not used	LPSS_UART_RTS/br i_dt	Can be shorted to A38 on the motherboard
55	LPSS_UART_RXD/b ri_rsp	N/C		Not used	LPSS_UART_RXD/b ri_rsp	Can be shorted to A39 on the motherboard
56	LPSS_UART_TXD/r gi_dt	N/C		Not used	LPSS_UART_TXD/r gi_dt	Can be shorted to A40 on the motherboard
57	LPSS_UART_CTS/rg i_rsp	N/C		Not used	LPSS_UART_CTS/rg i_rsp	Can be shorted to A41 on the motherboard



Electrical Specifications

Pin #	Pin Name platform pinout	Pin Name module pinout	Direction w/ respect to JfP Module	Function when CNVi is used	Function when Standard (discrete) M.2 is used	Comments
58	PCM_SYNC/I2S_WS	N/C		Not used	PCM_SYNC/I2S_WS	Can be shorted to A42 on the motherboard
59	PCM_OUT/I2S_SD_OUT	N/C		Not used	PCM_OUT/I2S_SD_OUT	Can be shorted to A43 on the motherboard
60	PCM_IN/I2S_SD_IN	N/C		Not used	PCM_IN/I2S_SD_IN	
61	PCM_CLK/I2S_SCK	N/C		Not used	PCM_CLK/I2S_SCK	
62	GND	GND		GND	GND	
63	W_DISABLE2#	W_DISABLE2#	I	W_DISABLE2#	W_DISABLE2#	This signal has an internal pull-up tied to 1.8V
64	LED2#	LED2#	O	LED2#	LED2#	
65	LED1#	LED1#	O	LED1#	LED1#	
66	RESERVED	RESERVED		Not used	RESERVED	
67	RESERVED	RESERVED		Not used	RESERVED	
68	GND	GND		GND	GND	
69	USB_D-	N/C		Not used	USB_D-	
70	USB_D+	N/C		Not used	USB_D+	
71	GND	GND		GND	GND	
72	3.3V	3.3V		3.3V	3.3V	
73	3.3V	3.3V		3.3V	3.3V	
74	GND	GND		GND	GND	
75	GND	GND		GND	GND	
76	GND	GND		GND	GND	
77	GND	GND		GND	GND	
78	GND	GND		GND	GND	
79	GND	GND		GND	GND	
80	GND	GND		GND	GND	
81	GND	GND		GND	GND	
82	GND	GND		GND	GND	
83	GND	GND		GND	GND	
84	GND	GND		GND	GND	
85	GND	GND		GND	GND	
86	GND	GND		GND	GND	



Electrical Specifications

Pin #	Pin Name platform pinout	Pin Name module pinout	Direction w/ respect to JfP Module	Function when CNVi is used	Function when Standard (discrete) M.2 is used	Comments
87	GND	GND		GND	GND	
88	GND	GND		GND	GND	
89	GND	GND		GND	GND	
90	GND	GND		GND	GND	
91	GND	GND		GND	GND	
92	GND	GND		GND	GND	
93	GND	GND		GND	GND	
94	GND	GND		GND	GND	
95	GND	GND		GND	GND	
96	GND	GND		GND	GND	
G1	GND	GND		GND	GND	
G2	GND	GND		GND	GND	
G3	GND	GND		GND	GND	
G4	GND	GND		GND	GND	
G5	GND	GND		GND	GND	Thermal pad
G6	GND	GND		GND	GND	Thermal pad
G7	GND	GND		GND	GND	Thermal pad
G8	GND	GND		GND	GND	Thermal pad
G9	GND	GND		GND	GND	Thermal pad
G10	GND	GND		GND	GND	Thermal pad
G11	GND	GND		GND	GND	Thermal pad
G12	GND	GND		GND	GND	Thermal pad
A07	GND	GND		GND	Not Applicable	
A08	A4WP_IRQ#	N/C		NC	Not Applicable	Not connected
A09	A4WP_CLK	N/C		NC	Not Applicable	Not connected
A10	A4WP_DATA	N/C		NC	Not Applicable	Not connected
A11	RESERVED	RESERVED		RESERVED	Not Applicable	Not connected
A12	RESERVED	RESERVED		RESERVED	Not Applicable	Not connected
A13	RESERVED	RESERVED		RESERVED	Not Applicable	Not connected
A14	RESERVED	RESERVED		RESERVED	Not Applicable	Not connected
A15	GND	LNA_EN		GND	Not Applicable	This a special purpose test pin of the JfP module Should be connected to Ground on the platform



Electrical Specifications

Pin #	Pin Name platform pinout	Pin Name module pinout	Direction w/ respect to JfP Module	Function when CNVi is used	Function when Standard (discrete) M.2 is used	Comments
A16	RESERVED	RESERVED		RESERVED	Not Applicable	Not connected
A17	RESERVED	RESERVED		RESERVED	Not Applicable	Not connected
A18	RESERVED	RESERVED		RESERVED	Not Applicable	Not connected
A19	WT_CLKP	WT_CLKP	I	WT_CLKP	Not Applicable	CNVio bus TX clock
A20	WT_CLKN	WT_CLKN	I	WT_CLKN	Not Applicable	CNVio bus TX clock
A21	WT_D0P	WT_D0P	I	WT_D0P	Not Applicable	CNVio bus TX lane 0
A22	WT_D0N	WT_D0N	I	WT_D0N	Not Applicable	CNVio bus TX lane 0
A23	WT_D1P	WT_D1P	I	WT_D1P	Not Applicable	CNVio bus TX lane 1
A24	WT_D1N	WT_D1N	I	WT_D1N	Not Applicable	CNVio bus TX lane 1
A25	C_P32K	C_P32K	I	Not Used	Not Applicable	Not used by Jefferson Peak
A26	GND	GND		GND	Not Applicable	
A27	RESERVED	RESERVED		RESERVED	Not Applicable	Not connected
A28	RESERVED	RESERVED		RESERVED	Not Applicable	Not connected
A29	RESERVED	RESERVED		RESERVED	Not Applicable	Not connected
A30	RESERVED	RESERVED		RESERVED	Not Applicable	Not connected
A31	GND	GND		GND	Not Applicable	
A32	WGR_CLKP	WGR_CLKP	O	WGR_CLKP	Not Applicable	CNVio bus RX clock
A33	WGR_CLKN	WGR_CLKN	O	WGR_CLKN	Not Applicable	CNVio bus RX clock
A34	WGR_D0P	WGR_D0P	O	WGR_D0P	Not Applicable	CNVio bus RX lane 0
A35	WGR_D0N	WGR_D0N	O	WGR_D0N	Not Applicable	CNVio bus RX lane 0
A36	WGR_D1P	WGR_D1P	O	WGR_D1P	Not Applicable	CNVio bus RX lane 1
A37	WGR_D1N	WGR_D1N	O	WGR_D1N	Not Applicable	CNVio bus RX lane 1
A38	BRI_DT	BRI_DT	I	BRI_DT	Not Applicable	BRI Bus Tx, Can be connected to 54 on the motherboard



Electrical Specifications

Pin #	Pin Name platform pinout	Pin Name module pinout	Direction w/respect to JfP Module	Function when CNVi is used	Function when Standard (discrete) M.2 is used	Comments
A39	BRI_RSP	BRI_RSP	O	BRI_RSP	Not Applicable	BRI Bus Rx, Can be connected to 55 on the motherboard
A40	RGI_DT	RGI_DT	I	RGI_DT	Not Applicable	RGI Bus Tx, Can be connected to 56 on the motherboard
A41	RGI_RSP	RGI_RSP	O	RGI_RSP	Not Applicable	RGI Bus Rx, Can be connected to 57 on the motherboard
A42	RF_RESET_B	RF_RESET_B	I	RF_RESET_B	Not Applicable	Jefferson peak RF (active low) Can be connected to 58 on the motherboard
A43	CLKREQ0	CLKREQ0	I	CLKREQ0	Not Applicable	Clock request for the 38.4MHz clock (CNVi reference clock), Can be connected to 59 on the motherboard
A44	REFCLK0	REFCLK0	O	REFCLK0	Not Applicable	38.4MHz clock from the JfP Module to the SoC
A45	NO CONNECT	NO CONNECT		NO CONNECT	Not Applicable	Pin must be left floating
A46	RESERVED	RESERVED		RESERVED	Not Applicable	Not connected
A47	RESERVED	RESERVED		RESERVED	Not Applicable	Not connected
A48	3.3V	3.3V		3.3V	Not Applicable	
A49	3.3V	3.3V		3.3V	Not Applicable	
A50	GND	GND		GND	Not Applicable	



Electrical Specifications

3.2 Input/output electrical specifications

Table 3-3 Input/Output electrical specifications

I/O type	Symbol	Parameter	Min	Max	Unit	Notes
1.8V I/O RF_RESET_B	V _{IH}	Input High Voltage	1.26	2.1	V	
	V _{IL}	Input Low Voltage	-0.3	0.54	V	
	R _{PU/PD}	Weak Pull-Up or Pull-Down	70	150	Kohm	
	I _{IN}	Input Leakage Current		10	uA	No Pull Up/Down
	V _{OH}	Output High Voltage	1.62	1.8	V	I _o = 2mA Load = 20pF
	V _{OL}	Output Low Voltage	0	0.18		I _o = 2mA Load = 20pF
	T _R , T _F	Rise, Fall Time		6	ns	Load = 20pF
	C _{IO}	IO Pin Capacitance		2	pF	
1.8V FS I/O A4WP_IRQ# A4WP_I2C_CLK A4WP_I2C_CLK (Note 1)	V _{IH}	Input High Voltage	1.26	2.1	V	
	V _{IL}	Input Low Voltage	-0.3	0.54	V	
	R _{PU/PD}	Weak Pull-Up or Pull-Down	100	180	Kohm	
	I _{IN}	Input Leakage Current		10	uA	No Pulls
	V _{OL} Push-Pull	Output Low Voltage Push-pull	0	0.36		I _o = 2mA Load = 50pF
	V _{OH} Push-Pull	Output Low Voltage Push-pull	1.62	1.8		I _o = 2mA Load = 50pF
	T _R , T _F Push-Pull	Rise, Fall Time Push-pull		18.5	ns	Load = 50pF
	V _{OL} Open Drain	Output Low Voltage	0	0.36		I _o = 2mA Load = 64pF RPU = 1Kohm
	C _{IO}	IO Pin Capacitance		2	pF	
1.8V FS_CR CLKREQ0 (Note 2)	V _{IH}	Input High Voltage	1.26	2.1	V	
	V _{IL}	Input Low Voltage	-0.3	0.54	V	
	R _{PU/PD}	Weak Pull-Up or Pull-Down	100	180	Kohm	
	I _{IN}	Input Leakage Current		10	uA	No Pulls
	V _{OH}	Output High Voltage	1.62	1.8	V	I _o = 2mA Load = 20pF
	V _{OL}	Output Low Voltage	0	0.18		I _o = 2mA Load = 20pF
	T _R , T _F	Rise, Fall Time		18.5	ns	Load = 20pF
	C _{IO}	IO Pin Capacitance		2	pF	



Electrical Specifications

I/O type	Symbol	Parameter	Min	Max	Unit	Notes
1.8V FS_3VT C_P32K (Note 3)	V _{IH}	Input High Voltage	1.26	2.1	V	
	V _{IL}	Input Low Voltage	-0.3	0.54	V	
	R _{PU/PD}	Weak Pull-Up or Pull-Down	150 (typical)		Kohm	
	I _{IN}	Input Leakage Current		10	uA	No Pulls
	V _{OH}	Output High Voltage	1.62	1.8	V	I _o = 1mA Load = 30pF
	V _{OL}	Output Low Voltage	0	0.18		I _o = 1mA Load = 30pF
	T _R , T _F	Rise, Fall Time		20	ns	Load = 30pF
	C _{IO}	IO Pin Capacitance		2	pF	
BRI and RGI 1.8V I/O BRI_DT BRI_RSP RGI_DT RGI_RSP (Note 4)	V _{IH}	Input High Voltage	1.26		V	
	V _{IL}	Input Low Voltage		0.54	V	
	R _{PU/PD}					
	I _{IN}					
	V _{OH}	Output High Voltage	1.62	1.8	V	50ohm driver impedance Load = 35pF
	V _{OL}	Output Low Voltage	0	0.18		
	T _R , T _F	Input Rise, Fall Time (V _{IL} to/from V _{IH} , 30/70%)		7	ns	
	T _R , T _F	Output Rise, Fall Time (V _{OL} to/from V _{OH} , 30/70%)		4	ns	
	R _b	Baud rate	4.8	76.8	Mbaud	Tolerance +/-5%
	C _{IO}	IO Pin Capacitance		2	pF	
CNVio (Note 5)	Signal parameters follow the MIPI D-PHY Specifications Rev1.1					

NOTES:

1. I2C max speed will be 1MHz (Fast plus Mode). I2C SDA & SCL I/Os must comply with 120ns max rise/fall time. I/O are protected against back-bias up to 1.8V and can withstand I/O voltage when the power supply is off.
2. I/O are protected against back-bias up to 1.98V and can withstand I/O voltage when the power supply is off.
3. Input is 3.6V tolerant. I/O are protected against back-bias up to 3.6V and can withstand I/O voltage when the power supply is off.
4. I/O are protected against back-bias up to 1.98V and can withstand I/O voltage when the power supply is off.
5. The D-PHY I/O pins must comply with the DC electrical specifications in "MIPI Alliance Specification for D-PHY Rev1.1." Specifically, the D-PHY JfP transmitter (JfP to Pulsar) DC characteristics are found in Section 9.1, Table 16. The D-PHY JfP receiver (Pulsar to JfP) DC characteristics are found in Section 9.2, Table 20.

3.3 Peak current consumption

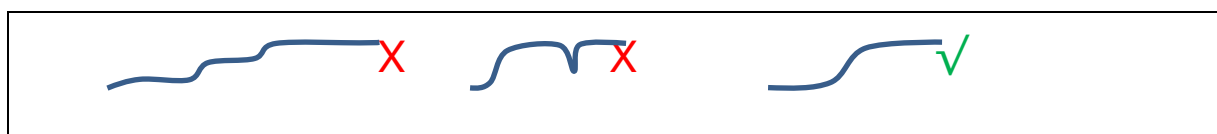
Table 3-4 Peak current consumption

Name	Description	Value [mA]	Notes
Peak current	Peak current from 3.3 V supply	1360	

3.4 M.2 power and ripple limits

The supply voltage rise should be continuous and with a max rise time of 10mSec (0 V to 3.3 V). It should not have any glitches or steps. Figure 3-1 shows examples of wrongful and correct power up schemes.

Figure 3-1 Power supply rise flow



3.4.1 Power supply ripples

There must not be any glitches on the power supply that dip more 0.3 V. Any glitch that is higher than 0.3V may be interpreted by the module as a *power-on reset*, which will cause the module to lose stored data and reboot.

During platform low-power modes, such as S3 (stand-by state), glitches will lead to connection failure.

Table 3-5 M.2 power supply and ripple limits

Platform Power Rail Requirements	
Power supply voltage range	3.3 V +/-0.165 V
Power on rise time	<10 msec
Maximum ripple	200 mVPP, frequency 10–500 kHz
Allowed power rail noise	300 mVpp

3.4.2 Platform state transitions

Platform designers should carefully design the transition from platform *on* state to platform *stand-by* state and vice versa, so that the power supply will remain stable and have no glitches.

3.5 M.2 ground (GND)

All ground pins are connected on the M.2 module to a common ground plane. The platform designer should connect all M.2 GND pins to the platform system GND.





4 Mechanical Specifications

Note: The module's mechanical specifications adhere to the *PCIe_M.2_Electromechanical_Spec.*

4.1 Weight

Table 4-1 Weight

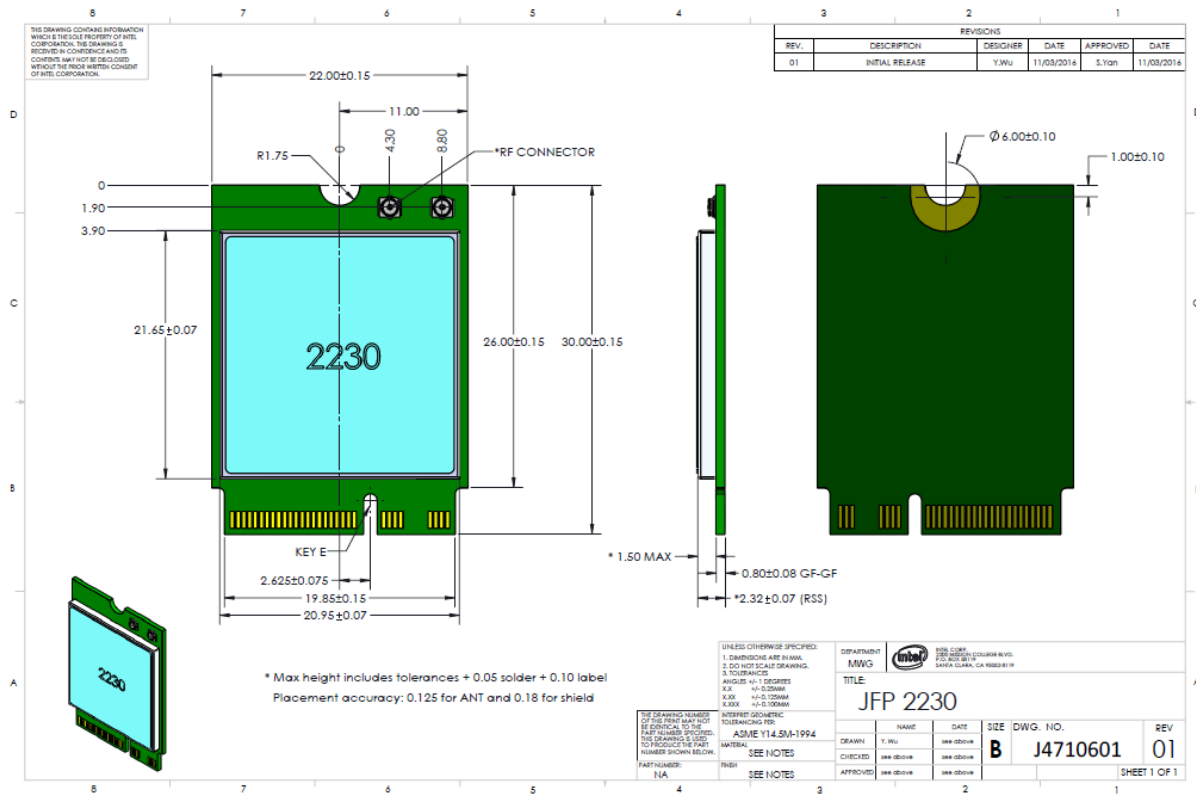
Product SKU	Size (mm × mm)	Weight (g)
Jefferson Peak 2230	22x30	2.5 +/- 0.25 grams
Jefferson Peak 1216	12x16	0.69 +/- 0.07g

4.2 M.2 2230 mechanical specification

Note: This section describes the mechanical specification of Jefferson Peak 2230 modules. Figure 4-1 shows the dimensions for type 2230. Antenna connector configuration and functionality for this form factor is listed in The shield dimensions in the drawing are taking into account the keep-out-zone required by the platform designers. The actual shield dimensions might be smaller than marked in the drawing.

Table 4-2 and shown in Figure 4-2.

Figure 4-1 Jefferson Peak M.2 2230 SKU dimensions



Note: The shield dimensions in the drawing are taking into account the keep-out-zone required by the platform designers. The actual shield dimensions might be smaller than marked in

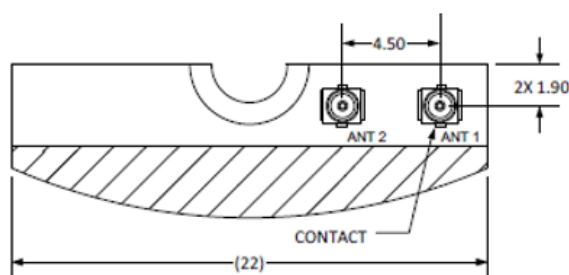
Mechanical Specifications

the drawing.

Table 4-2 Type 2230 antenna connector functionality

Antenna Connector 2230		
Function	PCIe* Spec Designation	Intel Module Label Designation
Wi-Fi (Chain A) + Bluetooth®	ANT1	1
Wi-Fi (Chain B)	ANT2	2

Figure 4-2 Jefferson Peak M.2 2230 SKU antenna configuration



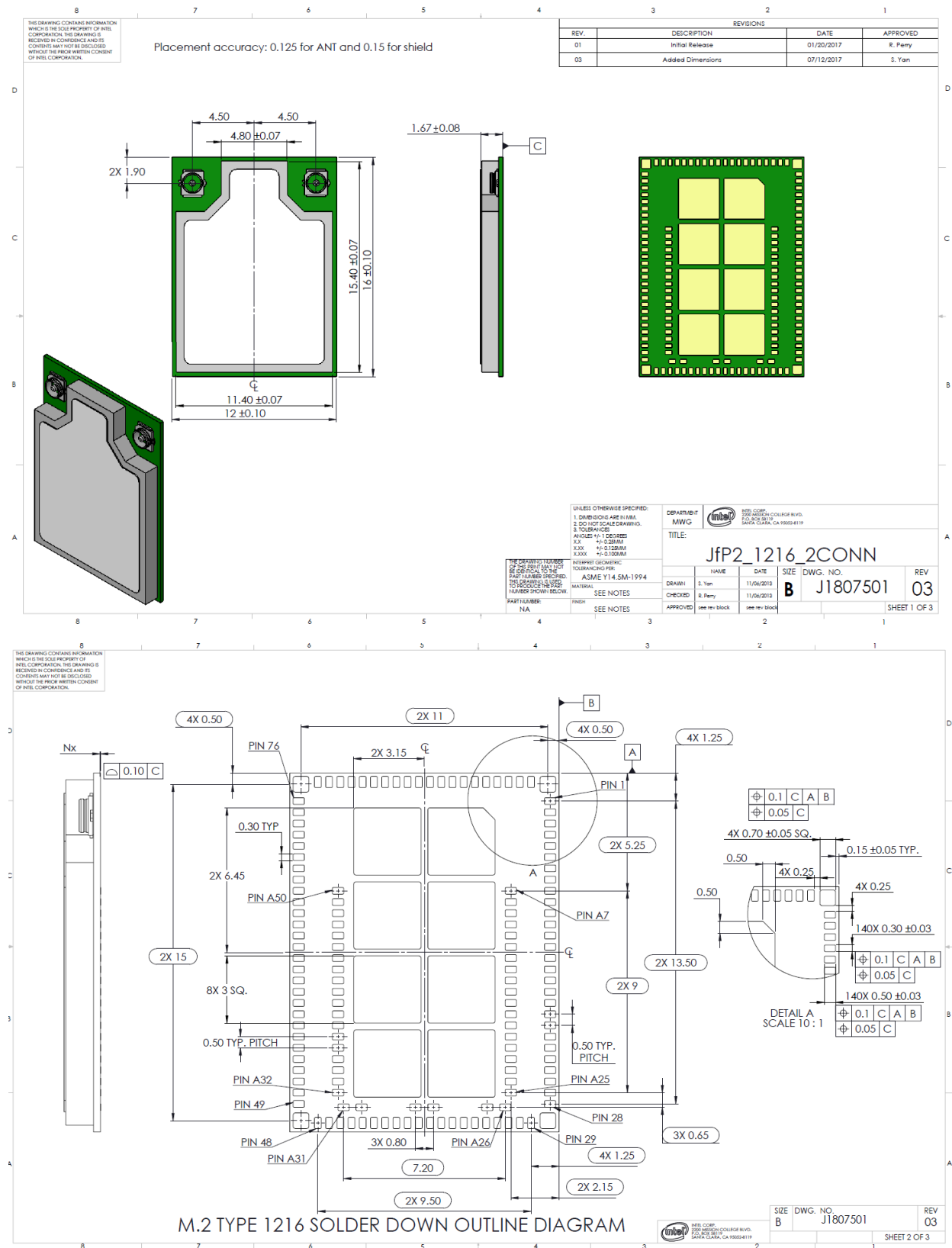
4.3 M.2 1216 mechanical specification

This section describes the mechanical specification of Jefferson Peak 2230 modules. Figure 4-3 shows the dimensions for type 1216 .Antenna connector configuration and functionality for this form factor is listed in Table 4-3 and shown in Figure 4-3.

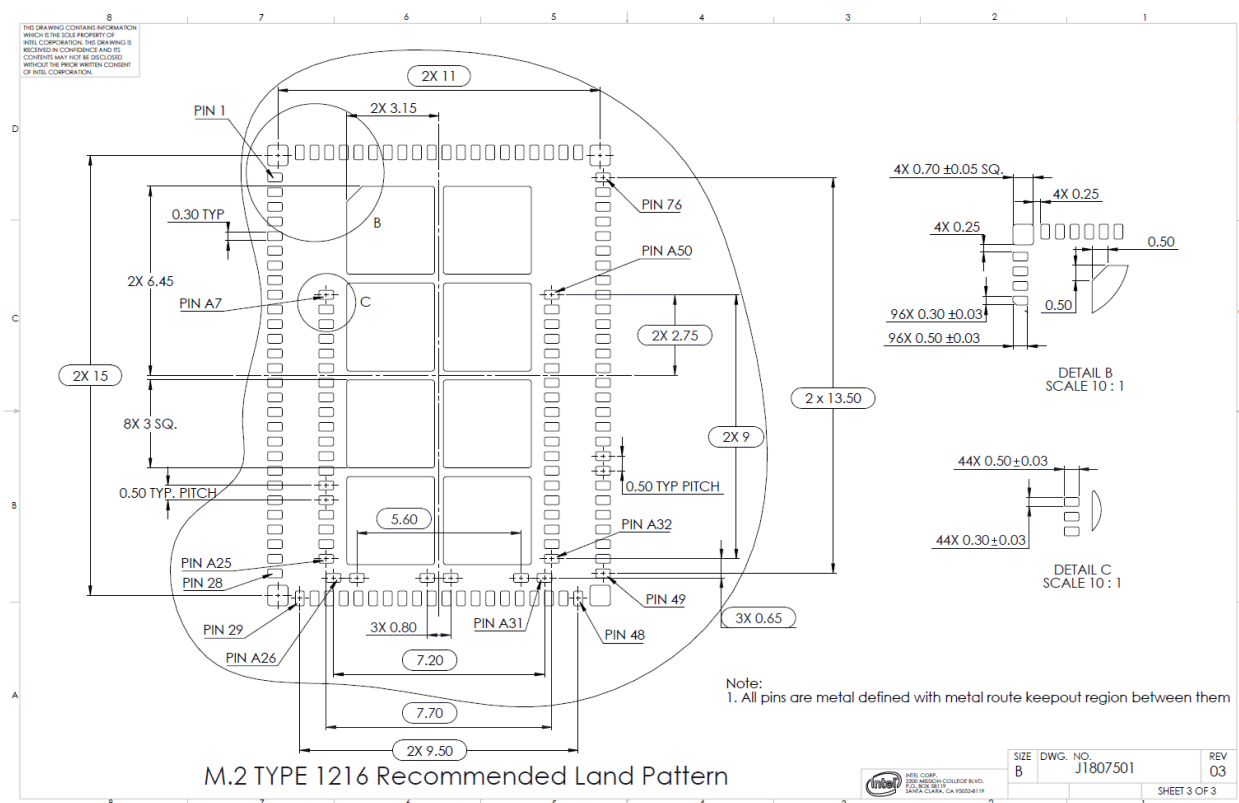


Mechanical Specifications

Figure 4-3 Jefferson Peak M.2 1216 SKU dimensions



Mechanical Specifications



Antenna connector functional allocation for this form factor is defined as shown in Table 4-3 (note the functionality is vendor-defined according to the M.2 spec).

Notes:

1. In Jefferson Peak 1216, antenna ANT2 is not present.
2. The PCB height of the M.2 1216 PCB is 0.3mm +/-10%.
3. The shield dimensions in the drawing are taking into account the keep-out-zone required by the platform designers. The actual shield dimensions might be smaller than marked in the drawing.

Table 4-3 Type 1216 antenna connector functionality

Antenna Connector 1216		
Function	PCIe* Spec Designation	Intel Module Label Designation
Wi-Fi (Chain A) + Bluetooth®	ANT1	1
Wi-Fi (Chain B)	ANT3	2



4.4 Z height

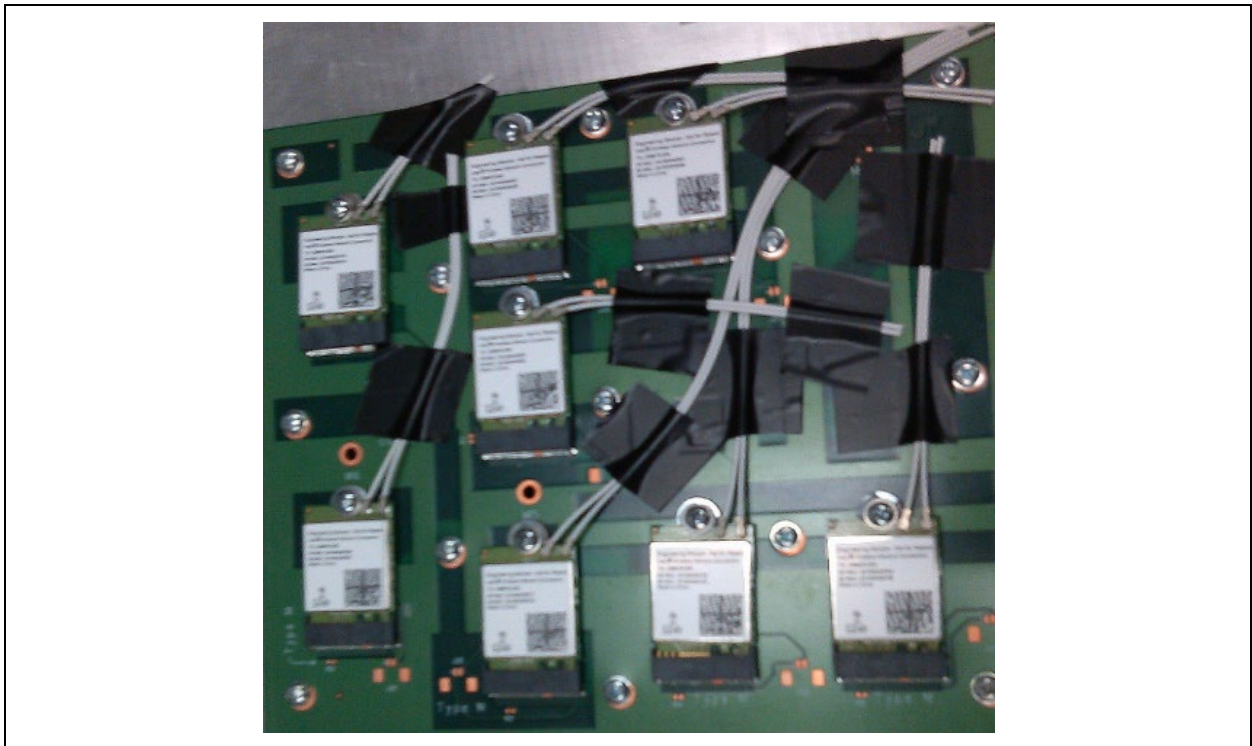
Jefferson Peak supports S3 Z-height module (1.5 mm from module surface to the top of the shield).

4.5 M.2 antenna retention

4.5.1 Recommended method for retention of M.2 cable

- It is recommended to restrain the antenna cables of M.2 products within the first 25 mm or less of cable length, leaving the RF connectors on the module.
- It is recommended to use a robust tape or adhesive to secure the cables so they do not move or pull on the RF connector during shock and vibration of the system, as shown in Figure 4-4.

Figure 4-4 Retention of M.2 cables



§



5 Performance

5.1 Power consumption

5.1.1 Wi-Fi power consumption

Table 5–1 Wi-Fi power consumption

Wi-Fi Power KPI	POR JfP2 [mW]
Unassociated	7.1
Idle associated 2.4GHz (consumer) DTIM=3 OOB	4.1
Idle associated 5.2GHz (enterprise) DTIM=1 OOB	4.9
Idle associated 2.4GHz (consumer) DTIM=3 benchmark Bluetooth® disabled No scan	3.7
Idle associated 5.2GHz (enterprise) DTIM=1 benchmark Bluetooth® disabled No scan	4.3
Web Browsing 2.4GHz (consumer)	14.2
Web Browsing 5.2GHz (enterprise)	16
VOIP 2.4GHz (consumer) NDP	265
VOIP 5.2GHz (enterprise) NDP	300
Video Conference 2.4GHz (consumer) NDP	270
Video Conference 5.2GHz (enterprise) NDP	320
Video Streaming 2.4GHz (consumer) NDP	35
Video Streaming 5.2GHz (enterprise) NDP	40
TpT – 11n LB-20 Tx 11n (at max TpT)	963
TpT – 11n LB-20 Rx 11n (at max TpT)	404
TpT – 11n HB-40 Tx 11n (at max TpT)	1021
TpT – 11n HB-40 Rx 11n (at max TpT)	550
TpT – 11ac HB-80 Tx 11ac (at max TpT)	1029



Wi-Fi Power KPI	POR JfP2 [mW]
TpT – 11ac HB-80 Rx 11ac (at max TpT)	650

NOTES:

1. Bluetooth® in SW RF-KILL in all the tests
2. Values measured in platform set to "Power Save Mode" enabled
3. OS: Win10
4. Clock sharing is not included in power consumption numbers. For Gemini Lake platform clock sharing adds 9mW to JfP power in Wi-Fi low power modes when the platform is in S0.

5.1.2 Bluetooth® power consumption

Table 5–2 Bluetooth® power consumption

Bluetooth® Power KPI	POR JfP2 [mW] Target
eSCO	39.4
MP3 playback Bluetooth® A2DP (at 345Kbps)	40.7
Continuous TX 10dBm	163.75
Continuous RX	111.02
HID Bluetooth® Low Energy connected idle	13.35
Bluetooth® Low Energy advertising	2.04
Bluetooth® Low Energy scanning	3.74
Page scan	5.73
Page and inquiry scan	7.84
BR/EDR sniff	6.1
OPP Tx (at max TpT)	100.04
OPP Rx (at max TpT)	101.71

NOTES:

1. Wi-Fi in SW RF-KILL in all the tests
2. OS: Win10
3. JfP is Master device
4. Clock sharing is not included in power consumption numbers. For the Gemini Lake platform, clock sharing adds 9mW to JfP power in Bluetooth® low-power modes when the platform is in S0.



Performance

5.2 Wi-Fi performance

5.2.1 Wi-Fi Tx power

Table 5–3 and Table 5–4 describe the device’s actual output power in various rates and channels, taking into account both Tx power regulatory limits and IEEE mask and EVM performance (the minimum between these). This is a change from previous generations of EPS documents.

Please note that the numbers in Table 5–3 and Table 5–4 are for the default location (before the actual location is determined), FCC countries, and ETSI countries. Also note that specific countries use combinations of ETSI and FCC regulatory limits per bands/sub-bands.

Table 5–3 JfP 2230 Tx power per MCS

JfP 2230 – 22.0 Values											
Expected accuracy of +/-1dB											
						Default [dBm]		ETSI (EU) [dBm]		FCC (US) [dBm]	
Modulation	Band	BW	Channel	Channel	MCS	SISO A	SISO B	SISO A	SISO B	SISO A	SISO B
.11b	LB	20MHz	2412	1	CCK11	15.5	15.5	15.5	15.5	18.75	19
.11b	LB	20MHz	2417	2	CCK11	15.5	15.5	15.5	15.5	19.75	20
.11b	LB	20MHz	2422	3	CCK11	15.5	15.5	15.5	15.5	19.88	19.5
.11b	LB	20MHz	2427	4	CCK11	15.5	15.5	15.5	15.5	20	20
.11b	LB	20MHz	2432	5	CCK11	15.5	15.5	15.5	15.5	20	20
.11b	LB	20MHz	2437	6	CCK11	15.5	15.5	15.5	15.5	20	20
.11b	LB	20MHz	2442	7	CCK11	15.5	15.5	15.5	15.5	20	20
.11b	LB	20MHz	2447	8	CCK11	15.5	15.5	15.5	15.5	20	20
.11b	LB	20MHz	2452	9	CCK11	15.5	15.5	15.5	15.5	20	20
.11b	LB	20MHz	2457	10	CCK11	15.5	15.5	15.5	15.5	20	20
.11b	LB	20MHz	2462	11	CCK11	15.5	15.5	15.5	15.5	19	20
.11b	LB	20MHz	2467	12	CCK11	15.5	15.5	15.5	15.5	17	17
.11b	LB	20MHz	2472	13	CCK11	14	13.75	15.5	15.5	14	13.75
.11g	LB	20MHz	2412	1	6	15	15.25	16	16	15	15.25
.11g	LB	20MHz	2412	1	54	13.5	14	16	16	13.5	14
.11g	LB	20MHz	2417	2	6	16	16	16	16	16.5	16.25
.11g	LB	20MHz	2417	2	54	15	14.75	16	16	15	14.75
.11g	LB	20MHz	2422	3	6	16	16	16	16	17.75	17.75
.11g	LB	20MHz	2422	3	54	16	16	15.75	16	16	16
.11g	LB	20MHz	2427	4	6	16	16	16	16	18	18
.11g	LB	20MHz	2427	4	54	16	15.88	16	16	16	16
.11g	LB	20MHz	2432	5	6	16	16	16	16	19	18.88



JfP 2230 – 22.0 Values											
Expected accuracy of +/-1dB											
						Default [dBm]		ETSI (EU) [dBm]		FCC (US) [dBm]	
Modulation	Band	BW	Channel	Channel	MCS	SISO A	SISO B	SISO A	SISO B	SISO A	SISO B
.11g	LB	20MHz	2432	5	54	15.88	16	16	16	16.13	16.5
.11g	LB	20MHz	2437	6	6	16	16	16	16	19	19.13
.11g	LB	20MHz	2437	6	54	16	16	15.88	16	16.5	16.75
.11g	LB	20MHz	2442	7	6	16	16	16	16	19.88	20
.11g	LB	20MHz	2442	7	54	15.88	16	16	16	16.38	17
.11g	LB	20MHz	2447	8	6	16	16	16	16	18.5	18.5
.11g	LB	20MHz	2447	8	54	15.88	16	16	16	16.25	16.38
.11g	LB	20MHz	2452	9	6	16	16	16	16	18	18
.11g	LB	20MHz	2452	9	54	16	16	16	16	16.25	16.25
.11g	LB	20MHz	2457	10	6	16	16	16	16	17	17.5
.11g	LB	20MHz	2457	10	54	15.75	16	16	16	15.75	16.25
.11g	LB	20MHz	2462	11	6	15.5	15.75	16	16	15.5	15.75
.11g	LB	20MHz	2462	11	54	14.5	14.5	16	16	14.5	14.5
.11g	LB	20MHz	2467	12	6	12.5	12.5	16	16	12.5	12.5
.11g	LB	20MHz	2467	12	54	11.5	12	16	16	11.5	12
.11g	LB	20MHz	2472	13	6	-6	-6	16	16	-6	-6
.11g	LB	20MHz	2472	13	54	-6	-6	16	16	-6	-6
.11n	LB	20MHz	2412	1	7	13.5	13.5	15.63	15.38	13.5	13.5
.11n	LB	20MHz	2417	2	7	15	14.5	15.75	15.5	15	14.5
.11n	LB	20MHz	2422	3	7	15.38	15.5	15.63	15.63	15.88	15.5
.11n	LB	20MHz	2427	4	7	15.5	15.5	15.75	15.63	15.88	15.5
.11n	LB	20MHz	2432	5	7	15.75	15.75	15.63	15.75	16	16
.11n	LB	20MHz	2437	6	7	15.75	15.88	15.63	15.63	16.38	16.25
.11n	LB	20MHz	2442	7	7	15.75	16	15.88	16	16.25	16.63
.11n	LB	20MHz	2447	8	7	15.75	16	15.88	16	16	16.5
.11n	LB	20MHz	2452	9	7	15.75	16	15.88	16	16	16.25
.11n	LB	20MHz	2457	10	7	15.75	16	16	16	15.75	16.25
.11n	LB	20MHz	2462	11	7	14	14.25	16	16	14	14.25
.11n	LB	20MHz	2467	12	7	11	11.75	16	16	11	11.75
.11n	LB	20MHz	2472	13	7	-6	-6	16	16	-6	-6
.11a	HB	20MHz	5180	36	6	14.5	14.5	16	16	16.5	17



Performance

JfP 2230 – 22.0 Values											
Expected accuracy of +/-1dB											
						Default [dBm]		ETSI (EU) [dBm]		FCC (US) [dBm]	
Modulation	Band	BW	Channel	Channel	MCS	SISO A	SISO B	SISO A	SISO B	SISO A	SISO B
.11a	HB	20MHz	5180	36	54	14.5	14.5	16	16	16	16.5
.11a	HB	20MHz	5200	40	6	14.5	14.5	16	16	19.5	19.75
.11a	HB	20MHz	5200	40	54	14.5	14.5	16	16	18.25	18.25
.11a	HB	20MHz	5220	44	6	14.5	14.5	16	16	20	19.88
.11a	HB	20MHz	5220	44	54	14.5	14.5	16	16	18.75	18.5
.11a	HB	20MHz	5240	48	6	14.5	14.5	16	16	20	20
.11a	HB	20MHz	5240	48	54	14.5	14.5	16	16	18.88	18.5
.11a	HB	20MHz	5260	52	6	14.5	14.5	16	16	20	20
.11a	HB	20MHz	5260	52	54	14.5	14.5	16	16	18.38	18.63
.11a	HB	20MHz	5280	56	6	14.5	14.5	16	16	19.75	20
.11a	HB	20MHz	5280	56	54	14.5	14.5	16	16	18.13	18.63
.11a	HB	20MHz	5300	60	6	14.5	14.5	16	16	19.5	20
.11a	HB	20MHz	5300	60	54	14.5	14.5	16	16	18	18.5
.11a	HB	20MHz	5320	64	6	14.5	14.5	16	16	16.5	16.5
.11a	HB	20MHz	5320	64	54	14.5	14.5	16	16	16	15.75
.11a	HB	20MHz	5500	100	6	16	16	16	16	16	17
.11a	HB	20MHz	5500	100	54	15.5	16	16	16	15.5	16.5
.11a	HB	20MHz	5520	104	6	16	16	16	16	19.5	19.75
.11a	HB	20MHz	5520	104	54	16	16	16	16	18	18.25
.11a	HB	20MHz	5785	157	6	13.5	13.5	16	16	20	20
.11a	HB	20MHz	5785	157	54	13.5	13.5	16	16	18.5	18.63
.11a	HB	20MHz	5805	161	6	13.5	13.5	16	16	20	20
.11a	HB	20MHz	5805	161	54	13.5	13.5	16	16	18.25	18.63
.11a	HB	20MHz	5825	165	6	13.5	13.5	16	16	19.5	19.75
.11a	HB	20MHz	5825	165	54	13.5	13.5	16	16	18	18.25
.11n	HB	20MHz	5180	36	7	14.5	14.5	16	16	15.5	16
.11n	HB	20MHz	5200	40	7	14.5	14.5	16	16	17.75	17.75
.11n	HB	20MHz	5500	100	7	15	16	16	16	15	16
.11n	HB	20MHz	5580	116	7	16	16	16	16	17.75	17.5
.11n	HB	20MHz	5825	165	7	13.5	13.5	16	16	17.5	17.25
.11ac	HB	20MHz	5200	40	8	14.5	14.5	16	16	17	17.25



JfP 2230 – 22.0 Values											
Expected accuracy of +/-1dB											
						Default [dBm]		ETSI (EU) [dBm]		FCC (US) [dBm]	
Modulation	Band	BW	Channel	Channel Index	MCS	SISO A	SISO B	SISO A	SISO B	SISO A	SISO B
.11ac	HB	20MHz	5500	100	8	14.5	15.5	16	16	14.5	15.5
.11ac	HB	20MHz	5805	161	8	13.5	13.5	15.75	15.75	16.75	17.13
.11n	HB	40MHz	5190	38	7	14	14	17	17	14	14
.11n	HB	40MHz	5230	46	7	15	15	17	17	18.5	17.88
.11n	HB	40MHz	5510	102	7	15	14.5	17	17	15	14.5
.11n	HB	40MHz	5795	159	7	13	13	17	17	18	17.5
.11ac	HB	40MHz	5230	46	9	14.38	14	15.63	15.75	16.13	15.63
.11ac	HB	40MHz	5510	102	9	14.75	14.5	15.5	15.63	14.75	14.5
.11ac	HB	40MHz	5795	159	9	12.63	13	14.75	15.38	14.75	15.25
.11ac	HB	80MHz	5210	42	9	13.5	13.38	14.63	14.25	14.25	13.75
.11ac	HB	80MHz	5530	106	9	12	10	12.38	10	12.75	10.5
.11ac	HB	80MHz	5775	155	9	12.25	12.25	14	14.38	14.25	14.5
.11ac	HB	160MHz	5250	50	9	10.75	10.75	12	11.88	10.75	11

NOTES:

1. The TX power per MCS relates to IEEE mask compliance and is limited by regulatory TX power limits.
2. The values relate to the internal FE SKU.
3. The values are for a typical device and typical conditions.

Table 5–4 JfP 1216 Tx power per MCS

JfP 1216 – 22.0 Values											
Expected accuracy of +/-1dB											
						Default [dBm]		ETSI (EU) [dBm]		FCC (US) [dBm]	
Modulation	Band	BW	Channel	Channel Index	MCS	SISO A	SISO B	SISO A	SISO B	SISO A	SISO B
.11b	LB	20MHz	2412	1	CCK11	15.5	15.5	15.5	15.5	18	18
.11b	LB	20MHz	2417	2	CCK11	15.5	15.5	15.5	15.5	19.5	19.38
.11b	LB	20MHz	2422	3	CCK11	15.5	15.5	15.5	15.5	19.88	19.38
.11b	LB	20MHz	2427	4	CCK11	15.5	15.5	15.5	15.5	19.63	19.25
.11b	LB	20MHz	2432	5	CCK11	15.5	15.5	15.5	15.5	19.63	19.38
.11b	LB	20MHz	2437	6	CCK11	15.5	15.5	15.5	15.5	19.5	19.25



Performance

JfP 1216 – 22.0 Values											
Expected accuracy of +/-1dB											
						Default [dBm]		ETSI (EU) [dBm]		FCC (US) [dBm]	
Modulation	Band	BW	Chan-nel	Channel Index	MCS	SISO A	SISO B	SISO A	SISO B	SISO A	SISO B
.11b	LB	20MHz	2442	7	CCK11	15.5	15.5	15.5	15.5	19.25	19.25
.11b	LB	20MHz	2447	8	CCK11	15.5	15.5	15.5	15.5	19.38	19
.11b	LB	20MHz	2452	9	CCK11	15.5	15.5	15.5	15.5	19.5	19.13
.11b	LB	20MHz	2457	10	CCK11	15.5	15.5	15.5	15.5	19.25	19.13
.11b	LB	20MHz	2462	11	CCK11	15.5	15.5	15.5	15.5	18.25	18.63
.11b	LB	20MHz	2467	12	CCK11	15.5	15.5	15.5	15.5	16.25	15.63
.11b	LB	20MHz	2472	13	CCK11	14.5	14.25	15.5	15.5	14.5	14.25
.11g	LB	20MHz	2412	1	6	15	15.5	16	16	15	15.5
.11g	LB	20MHz	2412	1	54	13.75	14	15.25	15.88	13.75	14
.11g	LB	20MHz	2417	2	6	16	16	16	16	16.5	16.5
.11g	LB	20MHz	2417	2	54	15.13	15.25	15.25	16	15.25	15.25
.11g	LB	20MHz	2422	3	6	16	16	16	16	17.75	18
.11g	LB	20MHz	2422	3	54	15.25	15.5	15.5	16	15.25	15.75
.11g	LB	20MHz	2427	4	6	16	16	16	16	18.25	18
.11g	LB	20MHz	2427	4	54	15.25	15.75	15.5	15.88	15.25	15.75
.11g	LB	20MHz	2432	5	6	16	16	16	16	18.25	18.38
.11g	LB	20MHz	2432	5	54	15.38	16	15.75	16	15.38	15.88
.11g	LB	20MHz	2437	6	6	16	16	16	16	18.38	18.38
.11g	LB	20MHz	2437	6	54	15.5	16	15.38	16	15.75	16
.11g	LB	20MHz	2442	7	6	16	16	16	16	18.38	18.38
.11g	LB	20MHz	2442	7	54	15.88	15.88	16	15.88	16	16
.11g	LB	20MHz	2447	8	6	16	16	16	16	17.75	18
.11g	LB	20MHz	2447	8	54	15.5	15.5	15.75	16	15.5	15.5
.11g	LB	20MHz	2452	9	6	16	16	16	16	17.75	18
.11g	LB	20MHz	2452	9	54	15.75	15.75	16	16	15.75	15.75
.11g	LB	20MHz	2457	10	6	16	16	16	16	17	17
.11g	LB	20MHz	2457	10	54	15.5	15.5	15.75	15.75	15.5	15.5
.11g	LB	20MHz	2462	11	6	15	15.5	16	16	15	15.5
.11g	LB	20MHz	2462	11	54	14	14.5	15.88	15.63	14	14.5
.11g	LB	20MHz	2467	12	6	12.5	12.5	16	16	12.5	12.5



JfP 1216 – 22.0 Values											
Expected accuracy of +/-1dB											
						Default [dBm]		ETSI (EU) [dBm]		FCC (US) [dBm]	
Modulation	Band	BW	Chan-nel	Channel Index	MCS	SISO A	SISO B	SISO A	SISO B	SISO A	SISO B
.11g	LB	20MHz	2467	12	54	11.5	11.75	15.88	15.75	11.5	11.75
.11g	LB	20MHz	2472	13	6	-6.5	-6.75	16	16	-6.5	-6.75
.11g	LB	20MHz	2472	13	54	-6.5	-6.75	15.88	15.75	-6.5	-6.75
.11n	LB	20MHz	2412	1	7	13	13.5	14.88	15	13	13.5
.11n	LB	20MHz	2417	2	7	15	15	15	15.38	15	15
.11n	LB	20MHz	2422	3	7	15.25	15	15.25	15.13	15.25	15
.11n	LB	20MHz	2427	4	7	15.25	14.75	15.25	15.13	15.25	15
.11n	LB	20MHz	2432	5	7	15.38	15.25	15.63	15.25	15.38	15.25
.11n	LB	20MHz	2437	6	7	15.63	15.13	15.63	15.25	15.63	15.38
.11n	LB	20MHz	2442	7	7	15.5	14.88	15.5	15.13	15.38	15.5
.11n	LB	20MHz	2447	8	7	15.25	14.75	15.38	15.25	15.25	14.75
.11n	LB	20MHz	2452	9	7	15.25	15	15.75	15.13	15.25	15
.11n	LB	20MHz	2457	10	7	15.25	14.75	15.5	15.13	15.25	14.75
.11n	LB	20MHz	2462	11	7	13.75	14	15.5	15.25	13.75	14
.11n	LB	20MHz	2467	12	7	11	11	15.13	14.88	11	11
.11n	LB	20MHz	2472	13	7	-6.5	-6.75	15.38	15	-6.5	-6.75
.11a	HB	20MHz	5180	36	6	14.5	14.5	16	16	17.25	16
.11a	HB	20MHz	5180	36	54	14.5	14.5	16	16	16.5	15.5
.11a	HB	20MHz	5200	40	6	14.5	14.5	16	16	19.75	19.5
.11a	HB	20MHz	5200	40	54	14.5	14.5	16	16	18.13	18.25
.11a	HB	20MHz	5220	44	6	14.5	14.5	16	16	19.63	20
.11a	HB	20MHz	5220	44	54	14.5	14.5	16	16	18.63	18.63
.11a	HB	20MHz	5240	48	6	14.5	14.5	16	16	19.88	19.75
.11a	HB	20MHz	5240	48	54	14.5	14.5	16	16	18.63	18.25
.11a	HB	20MHz	5260	52	6	14.5	14.5	16	16	20	20
.11a	HB	20MHz	5260	52	54	14.5	14.5	16	16	18.63	18.75
.11a	HB	20MHz	5280	56	6	14.5	14.5	16	16	20	20
.11a	HB	20MHz	5280	56	54	14.5	14.5	16	16	18.88	19
.11a	HB	20MHz	5300	60	6	14.5	14.5	16	16	19.75	20
.11a	HB	20MHz	5300	60	54	14.5	14.5	16	16	18.5	18.5



Performance

JfP 1216 – 22.0 Values											
Expected accuracy of +/-1dB											
						Default [dBm]		ETSI (EU) [dBm]		FCC (US) [dBm]	
Modulation	Band	BW	Chan-nel	Channel Index	MCS	SISO A	SISO B	SISO A	SISO B	SISO A	SISO B
.11a	HB	20MHz	5320	64	6	14.5	14.5	16	16	17.5	16.5
.11a	HB	20MHz	5320	64	54	14.5	14.5	16	16	16.5	16
.11a	HB	20MHz	5500	100	6	16	16	16	16	16.25	16.5
.11a	HB	20MHz	5500	100	54	15.75	16	16	16	15.75	16
.11a	HB	20MHz	5520	104	6	16	16	16	16	19.25	19.5
.11a	HB	20MHz	5520	104	54	16	16	16	16	18.25	18.25
.11a	HB	20MHz	5785	157	6	13.5	13.5	16	16	19.88	19.63
.11a	HB	20MHz	5785	157	54	13.5	13.5	16	16	18.38	17.88
.11a	HB	20MHz	5805	161	6	13.5	13.5	16	16	19.75	19.5
.11a	HB	20MHz	5805	161	54	13.5	13.5	16	16	18.13	17.88
.11a	HB	20MHz	5825	165	6	13.5	13.5	16	16	19.38	19.5
.11a	HB	20MHz	5825	165	54	13.5	13.5	16	16	18	17.75
.11n	HB	20MHz	5180	36	7	14.5	14.5	16	16	16.25	15
.11n	HB	20MHz	5200	40	7	14.5	14.5	16	16	18	17.88
.11n	HB	20MHz	5500	100	7	15.25	15.5	16	16	15.25	15.5
.11n	HB	20MHz	5580	116	7	16	16	16	16	18.38	18.13
.11n	HB	20MHz	5825	165	7	13.5	13.5	16	16	17.5	17
.11ac	HB	20MHz	5200	40	8	14.5	14.5	15.88	15.75	17	17
.11ac	HB	20MHz	5500	100	8	14.75	15	16	16	14.75	15
.11ac	HB	20MHz	5805	161	8	13.5	13.5	15.75	15.25	16.88	16.13
.11n	HB	40MHz	5190	38	7	14.75	15	16.5	16.5	14.75	15.25
.11n	HB	40MHz	5230	46	7	15	15	16.75	16.5	17.75	18
.11n	HB	40MHz	5510	102	7	13	12.75	17	16.88	13	12.75
.11n	HB	40MHz	5795	159	7	13	13	17	16.25	17.5	16.88
.11ac	HB	40MHz	5230	46	9	13.13	13	14.25	13.88	15.5	15.5
.11ac	HB	40MHz	5510	102	9	12.5	12.25	13	14.5	12.5	12.25
.11ac	HB	40MHz	5795	159	9	11.5	11.63	13.5	13	14	13.75
.11ac	HB	80MHz	5210	42	9	13.63	12.75	14.25	13.75	14.25	14.75
.11ac	HB	80MHz	5530	106	9	12.13	9.88	12	9.88	12.75	10.5
.11ac	HB	80MHz	5775	155	9	11.75	11.75	13.75	13.25	14.25	14



JfP 1216 – 22.0 Values											
Expected accuracy of +/-1dB											
						Default [dBm]		ETSI (EU) [dBm]		FCC (US) [dBm]	
Modulation	Band	BW	Chan-nel	Channel Index	MCS	SISO A	SISO B	SISO A	SISO B	SISO A	SISO B
.11ac	HB	160MHz	5250	50	9	10.88	10.13	12.13	11.13	12.75	12.5
.11ac	HB	160MHz	5570	114	9	10.5	10.5	11.38	11.13	10.5	10.5

NOTES:

1. The TX power per MCS relates to IEEE mask compliance and is limited by regulatory TX power limits.
2. The values relate to the internal FE SKU.
3. The values are for a typical device and typical conditions.

5.2.2 Wi-Fi sensitivity

Table 5–5 JfP2 2230 Wi-Fi sensitivity

				JfP 2230					
Band	Mode	BW [MHz]	Rate	Chain A [dBm, acc +/- 0.5 dB]			Chain B [dBm, acc +/- 0.5 dB]		
				LB	MHB	HHB	LB	MHB	HHB
LB	11b	20	CCK, 1Mbps	-96.5			-96.6		
		20	CCK, 11 Mbps	-89.1			-89		
	11g	20	Rate 6Mbps	-93.4			-93.3		
		20	Rate 12Mbps	-90.8			-90.8		
		20	Rate 54Mbps	-76			-76		
	11n LDPC	20	MCS0	-93.9			-93.7		
		20	MCS6	-77.4			-77.3		
		20	MCS7	-74.9			-74.8		
	11n LDPC	40	MCS0	-91.3			-91.1		
		40	MCS6	-74.5			-74.5		
		40	MCS7	-72.1			-72.2		
HB	11a	20	Rate 6Mbps	-93.6	-94.1	-93.9	93.9	-94.2	-94.2
		20	Rate 12Mbps	-91	-91.5	-91.4	-91.3	-91.6	-91.7
		20	Rate 54Mbps	-76.3	-76.7	-76.5	-76.5	-76.8	-76.8
		20	MCS0	-94.2	-94.7	-94.6	-94.5	-94.8	-94.8



Performance

				JfP 2230					
Band	Mode	BW [MHz]	Rate	Chain A [dBm, acc +/- 0.5 dB]			Chain B [dBm, acc +/- 0.5 dB]		
				LB	MHB	HHB	LB	MHB	HHB
	11n LDPC	20	MCS6	-77.7	-78.1	-77.9	-77.9	-78.2	-78.2
		20	MCS7	-75.1	-75.5	-75.4	-75.3	-75.6	-75.6
	11n LDPC	40	MCS0	-91.7	-92.3	-92.3	-92	-92.4	-92.6
		40	MCS6	-74.8	-75.2	-75	-75	-75.3	-75.2
		40	MCS7	-72.5	-72.9	-72.7	-72.7	-73	-73
	11ac LDPC	20	MCS0	-94.2	-94.6	-94.6	-94.5	-94.7	-94.7
		20	MCS8	-72.2	-72.5	-72.3	-72.3	-72.5	-72.6
	11ac LDPC	40	MCS0	-91.7	-92.2	-92.2	-92	-92.3	-92.5
		40	MCS8	-69.2	-69.6	-69.4	-69.5	-69.7	-69.8
		40	MCS9	-67.5	-68	-67.7	-67.8	-68.1	-68.1
	11ac LDPC	80	MCS0	-88.3	-88.8	-88.9	-88.6	-88.9	-89.1
		80	MCS7	-70.4	-70.8	-70.7	-70.8	-71.1	-71
		80	MCS8	-65.6	-66.1	-65.9	-65.9	-66.2	-66.1
		80	MCS9	-63.5	-63.9	-63.8	-63.6	-63.9	-63.9
	11ac LDPC	160	MCS0	-83.3	-83.5	-85.2	-84.4	-84.3	-85.5
		160	MCS7	-65.7	-66	-66	-66.1	-66.1	-66.1
		160	MCS8	-62.1	-62.4	-62.3	-62.4	-62.4	-62.2
		160	MCS9	-60	-60.1	-60	-60.3	-60.3	-59.8

NOTES:

1. Rx Power KPIs at antenna port over typical process/temperature/voltage
2. KPIs reflect 10% PER over AWGN channel, 1KB frame length, 1x1
3. LHB: Ch36-64, MHB: Ch100-144, HHB: Ch149-165

Table 5-6 JfP2 1216 Wi-Fi sensitivity

				JfP2 1216					
Band	Mode	BW [MHz]	Conditions	Chain A [dBm, acc +/- 0.5 dB]			Chain B [dBm, acc +/- 0.5 dB]		
				LB/LHB	MHB	HHB	LB/LHB	MHB	HHB
LB	11b	20	CCK, 1Mbps	-96.3			-95.8\ -94.7		
		20	CCK, 11 Mbps	-88.6			-88.2		
	11g	20	Rate 6Mbps	-93			-92.5		
		20	Rate 12Mbps	-90.4			-89.8		
		20	Rate 54Mbps	-75.7			-74.9		



				JfP2 1216					
Band	Mode	BW [MHz]	Conditions	Chain A [dBm, acc +/- 0.5 dB]			Chain B [dBm, acc +/- 0.5 dB]		
				LB/LHB	MHB	HHB	LB/LHB	MHB	HHB
	11n LDPC	20	MCS0	-93.4			-92.9		
		20	MCS6	-77			-76.5		
		20	MCS7	-74.4			-73.8		
	11n LDPC	40	MCS0	-90.8			-89.9		
		40	MCS6	-74.1			-73.7		
		40	MCS7	-71.8			-71.2		
HB	11a	20	Rate 6Mbps	-93.8	-94	-93.6	-94.1	-94	-93.9
		20	Rate 12Mbps	-91.3	-91.5	-91.2	-91.5	-91.5	-91.5
		20	Rate 54Mbps	-76.5	-76.7	-76.3	-76.7	-76.6	-76.6
	11n LDPC	20	MCS0	-94.3	-94.5	-94.1	-94.6	-94.5	-94.4
		20	MCS6	-77.9	-78.1	-77.7	-78.1	-78	-78
		20	MCS7	-75.4	-75.5	-75.2	-75.5	-75.5	-75.5
	11n LDPC	40	MCS0	-92	-92.2	-92	-92.2	-92.2	-92.3
		40	MCS6	-75	-75.2	-74.8	-75.2	-75	-75.1
		40	MCS7	-72.7	-72.9	-72.5	-72.8	-72.8	-72.8
	11ac LDPC	20	MCS0	-94.3	-94.4	-94	-94.6	-94.5	-94.4
		20	MCS8	-72.2	-72.5	-72	-72.5	-72.3	-72.4
	11ac LDPC	40	MCS0	-91.9	-92.1	-92	-92.2	-92.2	-92.2
		40	MCS8	-69.5	-69.6	-69.3	-69.6	-69.6	-69.6
		40	MCS9	-67.9	-68	-67.6	-68	-68	-67.9
	11ac LDPC	80	MCS0	-88.6	-88.8	-88.5	-88.7	-88.8	-89
		80	MCS7	-70.7	-70.8	-70.4	-71	-70.9	-71
		80	MCS8	-66	-66.1	-65.6	-66.2	-66.1	-66.1
		80	MCS9	-63.8	-63.9	-63.5	-63.8	-63.8	-63.7
	11ac LDPC	160	MCS0	-84.7	-84.7		-85	-84.7	
		160	MCS7	-66	-66.2		-66.4	-66.1	
		160	MCS8	-62.4	-62.5		-62.5	-62.4	
		160	MCS9	-60.4	-60.4		-60.5	-60.2	

NOTES:

1. Rx Power KPIs at antenna port over typical process/temperature/voltage
2. KPIs reflect 10% PER over AWGN channel, 1KB frame length, 1x1
3. LHB: Ch36-64, MHB: Ch100-144, HHB: Ch149-165



Performance

5.2.3 Wi-Fi throughput targets

Table 5-7 Wi-Fi throughput

Scenario	Description	Value [Mbps]	Notes
11n 20 MHz 2SS Rx	Conductive, best attenuation, UDP	128	
11n 20 MHz 2SS TX	Conductive, best attenuation, UDP	129	
11n 40 MHz 2SS Rx	Conductive, best attenuation, UDP	262	
11n 40 MHz 2SS TX	Conductive, best attenuation, UDP	258	
11ac 80 MHz 2SS Rx	Conductive, best attenuation, UDP	720	
11ac 80 MHz 2SS TX	Conductive, best attenuation, UDP	753	
11ac 160 MHz 2SS Rx	Conductive, best attenuation, UDP	1398	
11ac 160 MHz 2SS TX	Conductive, best attenuation, UDP/IP	1366	
11n 20 MHz 2SS Rx	Conductive, best attenuation, TCP/IP	124	
11n 20 MHz 2SS TX	Conductive, best attenuation, TCP/IP	116	
11n 40 MHz 2SS Rx	Conductive, best attenuation, TCP/IP	252	
11n 40 MHz 2SS TX	Conductive, best attenuation, TCP/IP	217	
11ac 80 MHz 2SS Rx	Conductive, best attenuation, TCP/IP	670	
11ac 80 MHz 2SS TX	Conductive, best attenuation, TCP/IP	650	
11ac 160 MHz 2SS Rx	Conductive, best attenuation, TCP/IP	1204	
11ac 160 MHz 2SS TX	Conductive, best attenuation, TCP/IP	1220	

Note: The throughput values relate to Intel® Cannon Lake Platform and CPU, Single User.

5.3 Bluetooth® performance

5.3.1 Bluetooth® Tx power

Table 5-8 Bluetooth® Tx power

Tx Power (dBm, acc: +/- 1.5 dB)			
	JfP2 2230	JfP2 1216	Notes
BR	9.5	9.2	Typical Conditions
EDR2	5.5	5.2	Typical Conditions
EDR3	5.5	5.2	Typical Conditions
BLE 1M	5.5	5.0	Typical Conditions
BLE LR	5.5	5.0	Typical Conditions
BLE 2M	5.5	5.0	Typical Conditions

Typical Operating Conditions are defined as:

- 1) Temperature of 25°C and nominal supply voltage.
- 2) The measured material is of typical process only.
- 3) The reported figure is the average power level over the frequency band.
- 4) For all measurements, the specified temperature is measured at the shield.



- 5) The power levels are specified at the product antenna port.
- 6) 1216 data applies to both LTE and Non-LTE SKUs.

5.3.2 Bluetooth® sensitivity

Table 5-9 Bluetooth® sensitivity

	2230 (dBm, acc: +/-2.0 dB)	1216 (dBm, acc: +/-2.0 dB)	Notes
BR	-93	-93	Typical Conditions
EDR2	-92	-92	Typical Conditions
EDR3	-85	-85	Typical Conditions
BLE 1M	-94	-94	Typical Conditions
BLE LR S=2	-98	-98	Typical Conditions
BLE LR S=8	-101.5	-101.5	Typical Conditions
BLE 2M	-89	-89	Typical Conditions

Typical Operating Conditions are defined as Nominal BQB test conditions. In addition, the following definitions apply:

- 1) Temperature of 25°C and nominal supply voltage.
- 2) The measured material is of typical process only.
- 3) The measurements are performed at spectrally clean (i.e., non-spur) channels.
- 4) For all measurements, the specified temperature is measured at the shield.
- 5) The sensitivity is specified at the product antenna port.
- 6) Assuming all co-located cores are disabled.
- 7) Averaged value across frequency.
- 8) 1216 data applies to both LTE and Non-LTE SKUs.

5.3.3 Bluetooth® throughput targets

This section details the Bluetooth® throughput.

The values are applicable to both 2230 and 1216 form factors.

- OPP throughput testing occurs in fully conductive environment.
- BTOE is a Broadcom 2070 card in an Intel NUC.
- Size of the file transferred is 3 MB and is tested three (3) times at each point.
- Wi-Fi and other cores are disabled. Bluetooth is connectable, not discoverable.

Table 5-10 Bluetooth® throughput targets

Test Type	Attenuation	Typical TPT [Kbps]
TX OPP	25-60db	1425
RX OPP	25-60db	1425





6 Thermal Specifications

Note: The numbers in this section are not final, and are subject to change.

6.1 Thermal dissipation

Maximum thermal dissipation is based on the assumption that both Wi-Fi and Bluetooth communication are active. Table 6–1 describes the thermal dissipation and targets per operated mode.

Customers who implement the CTD limits in their BIOS need to consider that values below 2000mW might limit the performance of the module (as a means to limit the thermal dissipation of the module).

The performance degradation due to CTD will mostly be seen when platform OS is not configured to “Power Save Mode” or when the Wi-Fi device transmits full Tx power.

Table 6–1 Thermal dissipation

Use Case		PC (mW)	
Wi-Fi	Bluetooth®	Wi-Fi	Bluetooth®
Worst case TDP: Based on average power consumption measurement over five minutes with max TCP/IP throughput activity		2000	150

Note: Not applicable for scenarios that may only be exercised using lab or OEM support software tools.

6.2 Thermal specifications

Table 6–2 Thermal management

Name	Description
Thermal shield performance targets	Full performance at shield temperatures up to 80 °C. Testing conditions: System environmental conditions: High limit: ~50 °C under controlled environment (oven), with no air flow (inside a box). Low limit: 0 °C (starting point) under controlled environment (oven), with no air flow (inside a box).
Thermal Silicon protection (CT–Kill)	Thermal silicon protection will not be activated below 85 °C T–shield temperature.

6.3 Thermal management

The device thermal management cuts off RF operation once a maximum temperature threshold (Critical Temperature termination, CT–Kill) has been exceeded. After the cutoff point is reached, the RF remains at the off state until it cools down to the thermal activation threshold. During this time the host cannot set the RF back to on.

When the product is heating up and nearing CT Kill, it will start decreasing the Wi-Fi activity in order to prevent the unit from heating further and reaching critical temperature. In such case, connectivity will be maintained but performance might be degraded gradually.



6.4 Module placement recommendations

The module disperses excess heat through the RF shield and the screws that ground the module to the chassis.

Correct module placement will ensure optimal thermal performance:

- The 2230 module orientation should be shield up.
- The 2230 module connection to chassis should be with a single metal screw. The connection screw shall be connected to the platform board ground.

6.5 Nonoperational module thermal storage

Table 6–3 Storage conditions

Environment	Limits
Storage Temperature (Non-Operational)	–40 °C to 70 °C
Humidity (Non-Operational)	50% to 90% non-condensing (at temperatures of 25 °C to 35 °C)





7 Regulatory

7.1 Regulatory channel support and output power

Jefferson Peak provides regulatory compliance via statically-configured SKUs or DRS (Dynamic Regulatory Solution).

For further details on the DRS scheme, refer to the DRS application note (see Section 8).

7.2 Wi-Fi channel configuration

7.2.1 Channel configuration – RF output power

The values listed in Table 5–3 represent the target power for the calibration process without antennae gain. This value has been verified to ensure margin from the regulatory limit based on post EEPROM factory calibration measurements using a diagnostic tool that operates the WLAN card at a ~99% DC (Duty Cycle) taken on both the main and auxiliary antenna ports.

As part of the factory test process, Intel measures the output power of every card. Any cards that exceed the maximum limits (EEPROM + 0.5dB) will not pass the factory test. While in operation, the card adjusts TX power using a closed-loop TX power calibration algorithm in concert with a power detector and temperature sensor.

Intel uses the following antenna gain value for product and country certification work: 3dBi for 2.4GHz and 5dBi for 5GHz.

Intel also incorporates a lower limit to ensure that compliance of the WLAN card is maintained. The minimum limits are set by factory processes.

7.2.2 Channel configuration – scan

Table 7–1 describes scan policies per sub-band and country setting.

Table 7–1 Scan policies per sub-band and country setting

	Channel Profile (0 = Disable, 1= Passive Scan, 2= Active Scan)								
	Sub-Band 2G4-A	Sub-Band 2G4-B	Sub-Band 5G2	Sub-Band 5G3	Sub-Band 5G4	Sub-Band 5G5	Sub-Band 5G8-A	Sub-Band 5G8-B	Sub-Band 5G9
	[25:24]	[27:26]	[29:28]	[31:30]	[33:32]	[35:34]	[37:36]	[39:28]	[41:40]
Default	2	2	1	1	0	1	1	1	0
FCC	2	2	1	1	0	1	2	1	0
USA TW	2	2	2	1	0	1	2	2	0
Canada IC	2	2	1	1	0	1	2	2	0
ETSI + 5G8SRD	2	2	1	1	0	1	2	2	0
Japan	2	2	1	1	0	1	1	1	0
Brazil	2	2	1	1	0	1	2	2	0
Indonesia	2	2	0	0	0	0	2	0	0
South Korea	2	2	1	1	0	1	2	2	0
Chile	2	2	1	1	0	1	2	1	0



7.2.3 Output power restrictions for main geographies

Table 7-2 Output power restrictions, main geographies

Output Power (dBm)							
Country/Geo	2.4 GHz	5.15 – 5.25 GHz	5.25 – 5.35 GHz	5.47 – 5.65 GHz	5.65 – 5.725 GHz	5.725 – 5.85 GHz	Unit
EU Countries EIRP	20	23	23	23 ³	23 ³	14 SRD	dBm
> EU Countries Cond. ^{1, 4}	17	18	18	18	18	9 SRD	dBm
United States ² Cond.	1000	250	250	250	250	1000	mW
> United States ² Cond.	30	24	24	24	24	30	dBm
Canada ² Cond.	1000	200 EIRP	250	250	250	1000	mW
Canada ² Cond.	30	23 EIRP	24	24	24	30	dBm
India	30	23 EIRP	23 EIRP	N/A	N/A	23 EIRP	dBm
China Cond.		18	18	24	24	27	dBm
China EIRP	20	23	23	30	30	33	dBm
Worst Case Cond. mW ²	100	50	200	250	250	100	mW
Worst Case Cond. dBm ¹	17	18	18	18	18	18	dBm

NOTES: Reference antenna gain: Max. Antenna Gain 3 dBi for 2.4 GHz and 5 dBi for 5 GHz

1. Assuming Max. Antenna Gain 3 dBi for 2.4 GHz and 5 dBi for 5 GHz
2. Allowance of up to a 6 dBi antenna allowed, if antenna is > 6 dBi output power must be reduced by 1 dB per dBi of antenna gain.
3. As DFS Slave Device (30 dBm for Master).
4. For Ukraine, the conducted value is the same as for the EU, assuming antenna peak gain is below 3dBi, EIRP should below 20dBm.

7.2.4 Channel configuration tables/RF output power

The values listed in the power table (EEPROM table) represent the target power for the calibration process without antennae gain. This value has been verified to ensure a margin from the regulatory limit based on post-EEPROM factory calibration measurements using a diagnostic tool that operates the WLAN card at a ~99% Duty Cycle (DC) taken on both the main and auxiliary antenna ports.

As part of the factory test process, Intel measures the output power of every card. Any cards that exceed the maximum limits (EEPROM + 0.5dB) will not pass the factory test. While in operation the card adjusts TX power using a closed loop TX power calibration algorithm. To do so, a power detector and temperature sensor are used. This algorithm adjusts the power to within +/-0.5 dB from the target, over temperature and voltage.

Intel uses the following antennae gain values for product and country certification work: 3dBi for 2.4GHz and 5dBi for 5GHz.

Intel also incorporates a lower limit to ensure that compliance of the WLAN card is maintained. The minimum limits are set by a factory process. In MIMO mode, this value is the sum limit. Generally if sum = 15 then Tx1 limit = 12 dBm and Tx2 limit = 12 dBm (exception for some channels according to the table below.)



Regulatory

7.3 Max Tx power

The product supports estimated max Tx power, as indicated in Table 7-3.

Notes:

1. Final numbers will be determined after the regulatory tests of the product are completed.
2. The values in the table relate to a single chain. It could happen that each chain transmits at that power at the same time.
3. The values indicate the worst case across channels and Tx modes. It may happen that in certain channels the max Tx power may be lower. Also when using high transmission rates the product will use lower Tx power.
4. The values in the table relate to the worst case absolute value that can be measured at the antenna port. For example, 20 dBm indicates 20 dBm at the antenna port. The device OTP might contain in that case value of 19 dBm to account for PA inaccuracy.

Table 7-3 Max Tx power

Band	Scenario	Value [dBm]	Notes
2.4 GHz	Max Tx power	21	
5 GHz	Max Tx power	21	

7.4 Tx power regulatory limits

7.4.1 About the regulatory tables

Please note the following:

- **DD**: Delay Diversity. *DD mode is currently NOT supported!*
- **BFer2**: *BFer mode is currently NOT supported!*
- Channel values in **red** indicate disabled channels.
- In some ETSI countries, SRD (Short Range Device) limits will kick in and reduce the Tx power below the ETSI values mentioned below. Specifically, ch 149-161 will be limited to 7.5dBm.

7.4.2 JfP2 2230 default max Tx power

Table 7-4 JfP2 2230 default max Tx power

JfP2 2230 Default 2.4GHz - 20MHz						
Central Freq.	Control / Central Channel	20MHz CCK		20MHz OFDM		
		SISO A	SISO B	SISO A	SISO B	MIMO 2
2412	1	15.50	15.50	15.50	15.50	10.00
2417	2	15.50	15.50	16.00	16.00	10.00
2422	3	15.50	15.50	16.00	16.00	10.00
2427	4	15.50	15.50	16.00	16.00	10.00
2432	5	15.50	15.50	16.00	16.00	10.00
2437	6	15.50	15.50	16.00	16.00	10.00
2442	7	15.50	15.50	16.00	16.00	10.00
2447	8	15.50	15.50	16.00	16.00	10.00
2452	9	15.50	15.50	16.00	16.00	10.00
2457	10	15.50	15.50	16.00	16.00	10.00



JfP2 2230 Default 2.4GHz - 20MHz						
Central Freq.	Control / Central Channel	20MHz CCK		20MHz OFDM		
		SISO A	SISO B	SISO A	SISO B	MIMO 2
2462	11	15.50	15.50	15.50	16.00	10.00
2467	12	15.50	15.50	13.00	12.50	10.00
2472	13	14.50	14.50	-6.50	-7.00	-8.50
2484	14	0	0	0	0	0

JfP 2.4GHz - 40MHz Default								
Central Freq.	Central channel	Control channel	Extension channel offset	40MHz CCK		40MHz OFDM		
				SISO A	SISO B	SISO A	SISO B	MIMO2
2422	3F	1	Above	15.50	15.50	14.50	14.00	12.50
		5	Below					
2427	4F	2	Above	15.50	15.50	15.50	15.50	13.00
		6	Below					
2432	5F	3	Above	15.50	15.50	15.50	15.50	13.00
		7	Below					
2437	6F	4	Above	15.50	15.50	15.50	15.50	13.00
		8	Below					
2442	7F	5	Above	15.50	15.50	15.00	15.00	13.00
		9	Below					
2447	8F	6	Above	15.50	15.50	15.50	15.50	13.00
		10	Below					
2452	9F	7	Above	15.50	15.50	14.00	13.50	12.50
		11	Below					
2457	10F	8	Above	15.50	15.50	10.50	10.00	10.00
		12	Below					
2462	11F	9	Above	14.50	14.50	2.50	3.00	2.00
		13	Below					



Regulatory

JFP 2230 5GHz - 20/40/80/160MHz Default																				
Control Channel	20MHz					40MHz					80MHz					160MHz				
	Central Frequency	Central Channel	SISO A	SISO B	MIMO2	Central Frequency	Central Channel	SISO A	SISO B	MIMO2	Central Frequency	Central Channel	SISO A	SISO B	MIMO2	Central Frequency	Central Channel	SISO A	SISO B	MIMO2
36	5180	24	14.50	14.50	11.50	5190	38F	15.00	15.00	12.00	5210	42ac80	15.00	15.00	12.00	5250	50AC160	13.00	13.00	11.00
40	5200	24	14.50	14.50	11.50															
44	5220	24	14.50	14.50	11.50															
48	5240	24	14.50	14.50	11.50															
52	5260	24	14.50	14.50	11.50	5270	54F	15.50	15.50	12.50	5290	58ac80	15.00	15.00	12.00	5330	70F			
56	5280	24	14.50	14.50	11.50															
60	5300	24	14.50	14.50	11.50															
64	5320	24	14.50	14.50	11.50															
68	5340	24				5390	78F				5370	74ac80				5410	82ac160			
72	5360	24																		
76	5380	24																		
80	5400	24																		
84	5420	24				5430	86F				5450	90ac80				5570	114ac160	14.50	14.50	13.00
88	5440	24																		
92	5460	24																		
96	5480	24																		
100	5500	24	16.00	16.00	13.00	5510	102F	16.50	16.00	14.00	5530	106ac80	17.00	16.50	13.50	5570	114ac160	14.50	14.50	13.00
104	5520	24	16.00	16.00	13.00															
108	5540	24	16.00	16.00	13.00															
112	5560	24	16.00	16.00	13.00															
116	5580	24	16.00	16.00	13.00	5590	118F	17.00	17.00	14.00	5610	122ac80	17.00	17.00	14.00	5690	138ac80	17.00	17.00	14.00
120	5600	24	16.00	16.00	13.00															
124	5620	24	16.00	16.00	13.00															
128	5640	24	16.00	16.00	13.00															
132	5660	24	16.00	16.00	13.00	5670	134F	17.00	17.00	14.00	5690	138ac80	17.00	17.00	14.00	5775	155ac80	13.00	13.00	10.00
136	5680	24	16.00	16.00	13.00															
140	5700	24	16.00	16.00	13.00															
144	5720	24	16.00	16.00	13.00															
149	5745	24	13.50	13.50	10.50	5755	151F	13.50	13.50	10.50	5775	155ac80	13.00	13.00	10.00	5815	163ac160			
153	5765	24	13.50	13.50	10.50															
157	5785	24	13.50	13.50	10.50															
161	5805	24	13.50	13.50	10.50															
165	5825	24	13.50	13.50	10.50	5835	167F				5855	171ac80				5815	163ac160			
169	5845	24																		
173	5865	24																		
177	5885	24																		
181	5905	24				5875	175F				NA	NA	NA	NA	NA	NA	NA	NA	NA	NA



7.4.3 JfP2 2230 FCC max Tx power

Table 7-5 JfP2 2230 FCC max Tx power

JfP2 FCC 2.4GHz - 20MHz						
Central Freq.	Control / Central Channel	20MHz CCK		20MHz OFDM		
		SISO A	SISO B	SISO A	SISO B	MIMO 2
2412	1	19.00	19.00	15.50	15.50	14.00
2417	2	20.00	20.00	17.00	18.00	15.00
2422	3	20.00	20.00	20.00	20.00	17.00
2427	4	20.00	20.00	20.00	20.00	17.00
2432	5	20.00	20.00	20.00	20.00	17.00
2437	6	20.00	20.00	20.00	20.00	17.00
2442	7	20.00	20.00	20.00	20.00	17.00
2447	8	20.00	20.00	20.00	20.00	17.00
2452	9	20.00	20.00	20.00	20.00	17.00
2457	10	20.00	20.00	18.00	18.00	16.00
2462	11	19.00	19.00	15.50	16.00	14.00
2467	12	18.00	18.00	13.00	12.50	10.50
2472	13	14.50	14.50	-6.50	-7.00	-8.50
2484	14					

JfP 2230 2.4GHz - 40MHz FCC								
Central Freq.	Central channel	Control channel	Extension channel offset	40MHz CCK		40MHz OFDM		
				SISO A	SISO B	SISO A	SISO B	MIMO2
2422	3F	1	Above	19.00	19.00	14.50	14.00	12.50
		5	Below					
2427	4F	2	Above	20.00	20.00	15.50	15.50	13.50
		6	Below					
2432	5F	3	Above	20.00	20.00	15.50	15.50	13.50
		7	Below					
2437	6F	4	Above	20.00	20.00	15.50	15.50	13.50
		8	Below					
2442	7F	5	Above	20.00	20.00	15.00	15.00	14.00
		9	Below					
2447	8F	6	Above	20.00	20.00	15.50	15.50	13.50
		10	Below					
2452	9F	7	Above	19.00	19.00	14.00	13.50	12.50
		11	Below					
2457	10F	8	Above	18.00	18.00	10.50	10.00	10.00
		12	Below					
2462	11F	9	Above	14.50	14.50	2.50	3.00	2.00
		13	Below					



Regulatory

JfP 2230 5GHz - 20/40/80/160MHz FCC																					
Control Channel	20MHz					Central Frequency	Central Channel	40MHz			Central Frequency	Central Channel	80MHz			Central Frequency	160MHz				
	Central Frequency	Central Channel	SISO A	SISO B	MIMO2			SISO A	SISO B	MIMO2			SISO A	SISO B	MIMO2		Central Channel	SISO A	SISO B	MIMO2	
36	5180	24	18.00	18.50	15.00	5190	38F	17.50	17.50	15.00	5210	42ac80	17.50	17.00	13.00	5250	50AC160	13.00	13.00	11.00	36
40	5200	24	19.50	20.00	18.00																40
44	5220	24	20.00	20.00	18.00																44
48	5240	24	20.00	20.00	18.00																48
52	5260	24	20.00	20.00	18.00	5270	54F	18.00	18.00	17.00	5290	58ac80	15.00	15.00	12.00	5330	62F	14.00	14.00	14.00	52
56	5280	24	20.00	20.00	18.00																56
60	5300	24	20.00	20.00	18.00																60
64	5320	24	15.50	16.00	15.00																64
68	5340	24				5350	70F				5370	74ac80				5410	82ac160				68
72	5360	24																			72
76	5380	24																			76
80	5400	24																			80
84	5420	24				5430	86F				5450	90ac80				5490	94F				84
88	5440	24																			88
92	5460	24																			92
96	5480	24																			96
100	5500	24	18.50	18.50	15.00	5510	102F	16.50	16.00	15.50	5530	106ac80	17.00	16.50	14.50	5570	114ac160	14.50	14.50	13.00	100
104	5520	24	20.00	20.00	18.00																104
108	5540	24	20.00	20.00	18.00																108
112	5560	24	20.00	20.00	18.00																112
116	5580	24	20.00	20.00	18.00	5590	118F	20.00	20.00	18.00	5610	122ac80	20.00	20.00	18.00	5650	126F	20.00	20.00	18.00	116
120	5600	24	20.00	20.00	18.00																120
124	5620	24	20.00	20.00	18.00																124
128	5640	24	20.00	20.00	18.00																128
132	5660	24	20.00	20.00	18.00	5670	134F	18.00	19.00	17.50	5690	138ac80	20.00	20.00	18.00	5730	138ac80	20.00	20.00	18.00	132
136	5680	24	20.00	20.00	18.00																136
140	5700	24	18.00	18.00	17.00																140
144	5720	24	19.50	19.00	17.00																144
149	5745	24	20.00	20.00	18.00	5755	151F	19.00	18.00	17.50	5775	155ac80	18.50	18.00	17.00	5815	163ac160				149
153	5765	24	20.00	20.00	18.00																153
157	5785	24	20.00	20.00	18.00																157
161	5805	24	20.00	20.00	18.00																161
165	5825	24	20.00	20.00	18.00	5795	159F	19.50	19.50	18.00	5835	167F				5875	171ac80				165
169	5845	24																			169
173	5865	24																			173
177	5885	24																			177
181	5905	24				5835	167F				5875	175F				5915	179F				181
185	5925	24				NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	185
189	5945	24				NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	189
193	5965	24				NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	193
197	5985	24				NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	197
201	6005	24				NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	201
205	6025	24				NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	205
209	6045	24				NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	209
213	6065	24				NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	213
217	6085	24				NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	217
221	6105	24				NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	221
225	6125	24				NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	225
229	6145	24				NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	229
233	6165	24				NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	233
237	6185	24				NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	237
241	6205	24				NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	241
245	6225	24				NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	245
249	6245	24				NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	249
253	6265	24				NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	253
257	6285	24				NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	257
261	6305	24				NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	261
265	6325	24				NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	265
269	6345	24				NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	269
273	6365	24				NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	273
277	6385	24				NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	277
281	6405	24				NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	281
285	6425	24				NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	285
289	6445	24				NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	289
293	6465	24				NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	293
297	6485	24				NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	297
301	6505	24				NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	301
305	6525	24				NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	305
309	6545	24				NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	309
313	6565	24				NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	313
317	6585	24				NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	317
321	6605	24				NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	321
325	6625	24				NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	325
329	6645	24				NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	329
333	6665	24				NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	333
337	6685	24				NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	337
341	6705	24				NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	341
345	6725	24				NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	345
349	6745	24				NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	349
353	6765	24				NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	353
357	6785	24				NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	357
361	6805	24				NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	361
365	6825	24				NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	365
369	6845	24				NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	369
373	6865	24				NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	373
377	6885	24				NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	377
381	6905	24				NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	381
385	6925	24				NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	385
389	6945	24				NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	389
393	6965	24				NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	393
397	6985	24				NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	397
401	7005	24				NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	401
405	7025	24				NA	NA	NA													



JfP 2230 2.4GHz - 40MHz ETSI								
Central Freq.	Central channel	Control channel	Extension channel offset	40MHz CCK		40MHz OFDM		
				SISO A	SISO B	SISO A	SISO B	MIMO2
2422	3F	1	Above	15.50	15.50	16.00	16.00	13.00
		5	Below					
2427	4F	2	Above	15.50	15.50	16.00	16.00	13.00
		6	Below					
2432	5F	3	Above	15.50	15.50	16.00	16.00	13.00
		7	Below					
2437	6F	4	Above	15.50	15.50	16.00	16.00	13.00
		8	Below					
2442	7F	5	Above	15.50	15.50	16.00	16.00	13.00
		9	Below					
2447	8F	6	Above	15.50	15.50	16.00	16.00	13.00
		10	Below					
2452	9F	7	Above	15.50	15.50	16.00	16.00	13.00
		11	Below					
2457	10F	8	Above	15.50	15.50	16.00	16.00	13.00
		12	Below					
2462	11F	9	Above	15.50	15.50	16.00	16.00	13.00
		13	Below					

JfP 2230 5GHz - 20/40/80/160MHz ETSI																					
Control Channel	20MHz					40MHz					80MHz					160MHz					
	Central Frequency	Central Channel	SISO A	SISO B	MIMO2	Central Frequency	Central Channel	SISO A	SISO B	MIMO2	Central Frequency	Central Channel	SISO A	SISO B	MIMO2		Central Frequency	Central Channel	SISO A	SISO B	MIMO2
36	5180	24	16.00	16.00	13.00	5190	38F	17.00	17.00	13.00	5210	42ac80	17.00	17.00	14.00		5250	50AC160	17.00	17.00	14.00
40	5200	24	16.00	16.00	13.00																
44	5220	24	16.00	16.00	13.00																
48	5240	24	16.00	16.00	13.00																
52	5260	24	16.00	16.00	13.00	5230	46F	17.00	17.00	13.00	5290	58ac80	17.00	17.00	14.00						
56	5280	24	16.00	16.00	13.00																
60	5300	24	16.00	16.00	13.00																
64	5320	24	16.00	16.00	13.00																
68	5340	24				5370	74ac80				5450	90ac80					5410	82ac160			
72	5360	24																			
76	5380	24																			
80	5400	24																			
84	5420	24				5430	86F				5470	94F									
88	5440	24																			
92	5460	24																			
96	5480	24																			
100	5500	24	16.00	16.00	13.00	5510	102F	17.00	17.00	14.00	5530	106ac80	17.00	16.50	13.50		5570	114ac160	17.00	17.00	14.00
104	5520	24	16.00	16.00	13.00																
108	5540	24	16.00	16.00	13.00																
112	5560	24	16.00	16.00	13.00																
116	5580	24	16.00	16.00	13.00	5590	118F	17.00	17.00	14.00	5610	122ac80	17.00	17.00	14.00						
120	5600	24	16.00	16.00	13.00																
124	5620	24	16.00	16.00	13.00																
128	5640	24	16.00	16.00	13.00																
132	5660	24	16.00	16.00	13.00	5630	126F	17.00	17.00	14.00	5690	138ac80	17.00	17.00	14.00						
136	5680	24	16.00	16.00	13.00																
140	5700	24	16.00	16.00	13.00																
144	5720	24	16.00	16.00	13.00																
148	5740	24	16.00	16.00	13.00	5710	142F	17.00	17.00	14.00	5775	155ac80	17.00	17.00	14.00						
152	5760	24	16.00	16.00	13.00																
156	5780	24	16.00	16.00	13.00																
160	5800	24	16.00	16.00	13.00																
164	5820	24	16.00	16.00	13.00	5755	151F	17.00	17.00	14.00	5855	171ac80					5815	163ac160			
168	5840	24																			
172	5860	24																			
176	5880	24																			
180	5900	24				5875	175F				NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA



Regulatory

7.4.5 JfP2 1216SD default max Tx power

Table 7-7 JfP2 1216SD default max Tx power

JfP2 1216 2.4GHz - 20MHz Default						
Central Freq.	Control / Central Channel	20MHz CCK		20MHz OFDM		
		SISO A	SISO B	SISO A	SISO B	MIMO 2
2412	1	15.50	15.50	15.00	15.50	13.00
2417	2	15.50	15.50	16.00	16.00	13.00
2422	3	15.50	15.50	16.00	16.00	13.00
2427	4	15.50	15.50	16.00	16.00	13.00
2432	5	15.50	15.50	16.00	16.00	13.00
2437	6	15.50	15.50	16.00	16.00	13.00
2442	7	15.50	15.50	16.00	16.00	13.00
2447	8	15.50	15.50	16.00	16.00	13.00
2452	9	15.50	15.50	16.00	16.00	13.00
2457	10	15.50	15.50	16.00	16.00	13.00
2462	11	15.50	15.50	15.00	15.50	13.00
2467	12	15.50	15.50	12.50	12.50	10.50
2472	13	14.50	14.25	-6.50	6.75	-9.00
2484	14					

JfP2 1216 2.4GHz - 40MHz								
Central Freq.	Central chann	Control channel	Extension channel offset	40MHz CCK		40MHz OFDM		
				SISO A	SISO B	SISO A	SISO B	MIMO2
2422	3F	1	Above	15.50	15.50	13.50	13.50	12.50
		5	Below					
2427	4F	2	Above	15.50	15.50	15.50	15.50	13.00
		6	Below					
2432	5F	3	Above	15.50	15.50	15.50	15.50	13.00
		7	Below					
2437	6F	4	Above	15.50	15.50	15.50	15.50	13.00
		8	Below					
2442	7F	5	Above	15.50	15.50	14.50	13.50	13.00
		9	Below					
2447	8F	6	Above	15.50	15.50	14.50	13.50	12.50
		10	Below					
2452	9F	7	Above	15.50	15.50	13.25	13.25	12.50
		11	Below					
2457	10F	8	Above	15.50	15.50	8.50	9.00	8.00
		12	Below					
2462	11F	9	Above	14.50	14.25	4.00	2.75	0.75
		13	Below					



JfP2 1216 5GHz - 20/40/80/160MHz																				
Control Channel	20MHz					40MHz					80MHz					160MHz				
	Central Frequency	Central Channel	SISO A	SISO B	MIMO2	Central Frequency	Central Channel	SISO A	SISO B	MIMO2	Central Frequency	Central Channel	SISO A	SISO B	MIMO2	Central Frequency	Central Channel	SISO A	SISO B	MIMO2
36	5180	24	14.50	14.50	11.50	5190	38F	15.00	15.00	12.00	5210	42ac80	15.00	15.00	8.50	5250	50AC160	15.00	15.00	12.00
40	5200	24	14.50	14.50	11.50															
44	5220	24	14.50	14.50	11.50	5270	54F	15.50	15.50	12.50	5310	62F	14.50	14.50	11.50	5350	70F			
48	5240	24	14.50	14.50	11.50															
52	5260	24	14.50	14.50	11.50	5430	86F				5450	90ac80								
56	5280	24	14.50	14.50	11.50															
60	5300	24	14.50	14.50	11.50	5510	102F	14.00	13.75	12.00	5530	106ac80	17.00	15.50	10.50	5570	114ac160	12.00	12.00	11.50
64	5320	24	14.50	14.50	11.50															
68	5340	24				5590	118F	17.00	17.00	14.00	5610	122ac80	17.00	17.00	14.00	5670	134F	17.00	17.00	14.00
72	5360	24																		
76	5380	24				5670	134F	17.00	17.00	14.00	5755	151F	13.50	13.50	10.50	5775	155ac80	13.00	13.00	10.00
80	5400	24																		
84	5420	24				5755	151F	13.50	13.50	10.50	5875	175F				5815	163ac160			
88	5440	24																		
92	5460	24				5835	167F				5855	171ac80								
96	5480	24																		
100	5500	24	16.00	16.00	13.00	5905	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA
104	5520	24	16.00	16.00	13.00															
108	5540	24	16.00	16.00	13.00	5905	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA
112	5560	24	16.00	16.00	13.00															
116	5580	24	16.00	16.00	13.00	5905	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA
120	5600	24	16.00	16.00	13.00															
124	5620	24	16.00	16.00	13.00	5905	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA
128	5640	24	16.00	16.00	13.00															
132	5660	24	16.00	16.00	13.00	5905	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA
136	5680	24	16.00	16.00	13.00															
140	5700	24	16.00	16.00	13.00	5905	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA
144	5720	24	16.00	16.00	13.00															
148	5740	24	13.50	13.50	10.50	5905	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA
152	5760	24	13.50	13.50	10.50															
156	5780	24	13.50	13.50	10.50	5905	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA
160	5800	24	13.50	13.50	10.50															
164	5820	24	13.50	13.50	10.50	5905	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA
168	5840	24																		
172	5860	24				5905	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA
176	5880	24																		
180	5900	24				NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA

7.4.6 JfP 1216SD FCC max Tx power

Table 7-8 JfP 1216SD FCC max Tx power

JfP2 1216 2.4GHz - 20MHz FCC						
Central Freq.	Control / Central Channel	20MHz CCK		20MHz OFDM		
		SISO A	SISO B	SISO A	SISO B	MIMO 2
2412	1	18.00	18.00	15.00	15.50	14.00
2417	2	20.00	20.00	17.00	17.00	15.00
2422	3	20.00	20.00	20.00	19.00	17.00
2427	4	20.00	20.00	20.00	19.00	17.00
2432	5	20.00	20.00	20.00	19.00	17.00
2437	6	20.00	20.00	20.00	19.00	17.00
2442	7	20.00	20.00	20.00	19.00	17.00
2447	8	20.00	20.00	20.00	19.00	17.00
2452	9	20.00	20.00	20.00	19.00	17.00
2457	10	20.00	20.00	17.00	17.00	15.00
2462	11	18.75	19.00	15.00	15.50	14.00
2467	12	16.25	16.25	12.50	12.50	10.50
2472	13	14.50	14.25	-6.50	6.75	-9.00
2484	14					



Regulatory

JfP2 1216 2.4GHz - 40MHz FCC								
Central Freq.	Central chann	Control channel	Extension channel offset	40MHz CCK		40MHz OFDM		
				SISO A	SISO B	SISO A	SISO B	MIMO2
2422	3F	1	Above	18.00	18.00	13.50	13.50	12.50
		5	Below					
2427	4F	2	Above	20.00	20.00	15.50	15.50	14.00
		6	Below					
2432	5F	3	Above	20.00	20.00	15.50	15.50	14.00
		7	Below					
2437	6F	4	Above	20.00	20.00	15.50	15.50	14.00
		8	Below					
2442	7F	5	Above	20.00	20.00	14.50	13.50	13.75
		9	Below					
2447	8F	6	Above	20.00	20.00	14.50	13.50	12.50
		10	Below					
2452	9F	7	Above	18.75	19.00	13.25	13.25	12.50
		11	Below					
2457	10F	8	Above	16.25	16.25	8.50	9.00	8.00
		12	Below					
2462	11F	9	Above	14.50	14.25	4.00	2.75	0.75
		13	Below					

JfP2 1216 5GHz - 20/40/80/160MHz FCC																					
Control Channel	20MHz					40MHz					80MHz					160MHz					
	Central Frequency	Central Channel	SISO A	SISO B	MIMO2	Central Frequency	Central Channel	SISO A	SISO B	MIMO2	Central Frequency	Central Channel	SISO A	SISO B	MIMO2	Central Frequency	Central Channel	SISO A	SISO B	MIMO2	Bfer
36	5180	24	17.25	16.00	15.00	5190	38F	18.75	18.75	13.50	5210	42ac80	17.50	16.50	8.50	5250	50AC160	15.00	15.50	12.00	12.00
40	5200	24	20.00	20.00	17.75																
44	5220	24	20.00	20.00	18.00																
48	5240	24	20.00	20.00	17.50																
52	5260	24	20.00	20.00	18.00	5270	54F	20.00	20.00	17.75	5290	58ac80	14.00	14.00	11.00	5410	82ac160				
56	5280	24	20.00	20.00	18.00																
60	5300	24	20.00	20.00	18.00																
64	5320	24	17.50	16.50	15.00																
68	5340	24				5350	70F				5370	74ac80				5410	82ac160				
72	5360	24																			
76	5380	24																			
80	5400	24																			
84	5420	24				5430	86F				5450	90ac80				5410	82ac160				
88	5440	24																			
92	5460	24																			
96	5480	24																			
100	5500	24	16.25	16.50	15.25	5510	102F	14.00	13.75	12.00	5530	106ac80	18.00	15.50	10.50	5570	114ac160	12.00	12.00	11.50	11.50
104	5520	24	20.00	20.00	18.00																
108	5540	24	20.00	20.00	18.00																
112	5560	24	20.00	20.00	18.00																
116	5580	24	20.00	20.00	18.00	5590	118F	17.00	17.00	16.00	5610	122ac80	18.00	17.50	17.00	5690	138ac80	19.00	19.50	19.00	
120	5600	24	20.00	20.00	17.00																
124	5620	24	20.00	20.00	18.00																
128	5640	24	20.00	20.00	18.00																
132	5660	24	20.00	20.00	18.00	5630	126F	17.00	17.00	16.00	5670	134F	19.00	18.00	16.50	5690	138ac80	19.00	19.50	19.00	
136	5680	24	20.00	20.00	18.00																
140	5700	24	18.00	18.00	17.00																
144	5720	24	20.00	20.00	19.00																
149	5745	24	20.00	20.00	19.00	5710	142F	19.50	20.00	19.25	5775	155ac80	16.00	15.50	13.00	5815	163ac160				
153	5765	24	20.00	20.00	19.00																
157	5785	24	20.00	20.00	19.00																
161	5805	24	20.00	20.00	19.00																
165	5825	24	20.00	20.00	19.00	5795	159F	20.00	20.00	19.00	5855	171ac80				5815	163ac160				
169	5845	24																			
173	5865	24																			
177	5885	24																			
181	5905	24				5835	167F				5855	171ac80				5815	163ac160				
						5875	175F														
						NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA

**7.4.7 JfP 1216SD ETSI max Tx power****Table 7–9 JfP 1216SD ETSI max Tx power**

JfP2 1216 2.4GHz - 20MHz ETSI						
Central Freq.	Control / Central Channel	20MHz CCK		20MHz OFDM		
		SISO A	SISO B	SISO A	SISO B	MIMO 2
2412	1	15.50	15.50	16.00	16.00	13.00
2417	2	15.50	15.50	16.00	16.00	13.00
2422	3	15.50	15.50	16.00	16.00	13.00
2427	4	15.50	15.50	16.00	16.00	13.00
2432	5	15.50	15.50	16.00	16.00	13.00
2437	6	15.50	15.50	16.00	16.00	13.00
2442	7	15.50	15.50	16.00	16.00	13.00
2447	8	15.50	15.50	16.00	16.00	13.00
2452	9	15.50	15.50	16.00	16.00	13.00
2457	10	15.50	15.50	16.00	16.00	13.00
2462	11	15.50	15.50	16.00	16.00	13.00
2467	12	15.50	15.50	16.00	16.00	13.00
2472	13	15.50	15.50	16.00	16.00	13.00
2484	14					

JfP2 1216 2.4GHz - 40MHz ETSI								
Central Freq.	Central chann	Control channel	Extension channel offset	40MHz CCK		40MHz OFDM		
				SISO A	SISO B	SISO A	SISO B	MIMO2
2422	3F	1	Above	15.50	15.50	16.00	16.00	13.00
		5	Below					
2427	4F	2	Above	15.50	15.50	16.00	16.00	13.00
		6	Below					
2432	5F	3	Above	15.50	15.50	16.00	16.00	13.00
		7	Below					
2437	6F	4	Above	15.50	15.50	16.00	16.00	13.00
		8	Below					
2442	7F	5	Above	15.50	15.50	16.00	16.00	13.00
		9	Below					
2447	8F	6	Above	15.50	15.50	16.00	16.00	13.00
		10	Below					
2452	9F	7	Above	15.50	15.50	16.00	16.00	13.00
		11	Below					
2457	10F	8	Above	15.50	15.50	16.00	16.00	13.00
		12	Below					
2462	11F	9	Above	15.50	15.50	16.00	16.00	13.00
		13	Below					



Regulatory

JfP2 1216 5GHz - 20/40/80/160MHz ETSI																					
Control Channel	20MHz					40MHz					80MHz					160MHz					Bfer
	Central Frequency	Central Channel	SISO A	SISO B	MIMO2	Central Frequency	Central Channel	SISO A	SISO B	MIMO2	Central Frequency	Central Channel	SISO A	SISO B	MIMO2	Central Frequency	Central Channel	SISO A	SISO B	MIMO2	
36	5180	24	16.00	16.00	13.00	5190	38F	17.00	17.00	13.00	5210	42ac80	17.00	17.00	14.00	5250	50AC160	17.00	17.00	14.00	11.00
40	5200	24	16.00	16.00	13.00																
44	5220	24	16.00	16.00	13.00																
48	5240	24	16.00	16.00	13.00																
52	5260	24	16.00	16.00	13.00	5270	54F	17.00	17.00	13.00	5290	58ac80	17.00	17.00	14.00	5310	62F	17.00	17.00	13.00	
56	5280	24	16.00	16.00	13.00																
60	5300	24	16.00	16.00	13.00																
64	5320	24	16.00	16.00	13.00																
68	5340	24				5350	70F				5370	74ac80				5410	82ac160				
72	5360	24																			
76	5380	24																			
80	5400	24																			
84	5420	24				5390	78F				5450	90ac80				5410	82ac160				
88	5440	24																			
92	5460	24																			
96	5480	24																			
100	5500	24	16.00	16.00	13.00	5510	102F	17.00	17.00	14.00	5530	106ac80	17.00	16.50	13.50	5570	114ac160	17.00	17.00	14.00	11.00
104	5520	24	16.00	16.00	13.00																
108	5540	24	16.00	16.00	13.00																
112	5560	24	16.00	16.00	13.00																
116	5580	24	16.00	16.00	13.00	5590	118F	17.00	17.00	14.00	5610	122ac80	17.00	17.00	14.00	5630	126F	17.00	17.00	14.00	
120	5600	24	16.00	16.00	13.00																
124	5620	24	16.00	16.00	13.00																
128	5640	24	16.00	16.00	13.00																
132	5660	24	16.00	16.00	13.00	5670	134F	17.00	17.00	14.00	5690	138ac80	17.00	17.00	14.00	5710	142F	17.00	17.00	14.00	
136	5680	24	16.00	16.00	13.00																
140	5700	24	16.00	16.00	13.00																
144	5720	24	16.00	16.00	13.00																
149	5745	24	16.00	16.00	13.00	5755	151F	17.00	17.00	14.00	5775	155ac80	17.00	17.00	14.00	5795	159F	17.00	17.00	14.00	
153	5765	24	16.00	16.00	13.00																
157	5785	24	16.00	16.00	13.00																
161	5805	24	16.00	16.00	13.00																
165	5825	24	16.00	16.00	13.00	5835	167F				5855	171ac80				5815	163ac160				
169	5845	24																			
173	5865	24																			
177	5885	24																			
181	5905	24				5875	175F									5815	163ac160				
						NA		NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	

7.5 SAR Tx power limits

OEMs who implement SAR limitations on their platforms can use the values in Table 7-10 for Tx power limits based on antenna-to-human body separation distance. Using the limits below will enable OEMs to have minimized C1PC paperwork. In the case of shorter distances, specific platform tests and a C2PC approval process will be needed.

Table 7-10 SAR Tx power limits dependency on distance

d = Antenna to Human Body Separation [mm]	Value [dBm] for Both Chain A and B acc: +/- 0.5dB		Required OEM SAR Regulatory Process
	2.4GHz	5GHz	
d >= 15	No need for BIOS SAR limits		None
8 <= d < 18	17.5	16	C1PC
5 <= d < 8	15	13.5	C1PC
<5	OEM to set specific BIOS SAR limits		C2PC

Note:

- The values in the table are per chain. Both chains can transmit at the stated power simultaneously.
- The C1PC process is allowed only if the same antenna "Type" has already been filed. If, for any reason, an OEM files for a new antenna "Type," the C2PC process is required even if the TX power falls within the limits.



7.6 Regulatory and safety certification

The following regulatory and safety information is subject to change.

Table 7–11 Wi-Fi safety and regulatory USA

USA	Requirements	Criteria
	EMI	FCC Part 15, Subpart B, Class B (CISPR 22 limits at 10 m)
	RF	FCC Part 15, Subpart C (Sections 15.205, 15.207, 15.209, and 15.247) FCC Part 15, Subpart E (Section 15.407)
	Safety	UL 60950–1

Table 7–12 Wi-Fi safety and regulatory Europe

Europe	Requirements	Criteria
	EMC	EN301489–1, EN 301489–17
	RF	EN300 328, EN300 440 and EN301–893 as DFS slave terminal
	Safety	EN60950–1 via CB Report (IEC60950–1) R&TTE Health Requirement referring to the EN 50566–2013 and 62209–2:2010

Table 7–13 Wi-Fi safety and regulatory Japan

Japan	Requirements	Criteria
	EMI	VCCI Class B
	RF	STD T66, STD T71, ARIB W52, W53, W56
	Safety	EN60950–1 via CB Report (IEC60950–1) R&TTE Health Requirement referring to the EN 50566–2013 and 62209–2:2010

Table 7–14 Wi-Fi safety and regulatory Australia/New Zealand

Australia/ New Zealand	Requirements	Criteria
	EMC	EU test reports
	RF	Radio communications (EMR) Standard 2003; EU test reports + Delta AS–NZ4268
	Safety	CB Cert. and Report (IEC60950–1)



Regulatory

Table 7–15 Wi-Fi safety and regulatory other geographies

Other Geographies	Requirements	Criteria
	Priority 2 Countries	To be covered in MWG Regulatory WW Country Coverage
	Priority 3 Countries	To be covered in MWG Regulatory WW Country Coverage

Note: Regulatory pre-scans and certification are tested using a combo Bluetooth®/Wi-Fi reference antenna.





8 Dynamic Regulatory Solution

8.1 Overview

Beginning with the Intel® Dual Band Wireless 7265 module (Stone Peak 2 or StP2), Intel® introduces a new Dynamic Regulatory Solution (DRS), which offers worldwide regulatory compliance on one hardware SKU while offering optimizations to country regulations based on geo-location discovery. These Wi-Fi optimizations include the following benefits:

- Robust regulatory compliance
- A single, worldwide regulatory hardware SKU
- Country-specific channel optimizations
- Minimized OEM effort on enablement, production, and inventory management
- Ability to meet changing regulations and field support with software updates
- Simpler worldwide procurement and distribution for enterprise customers

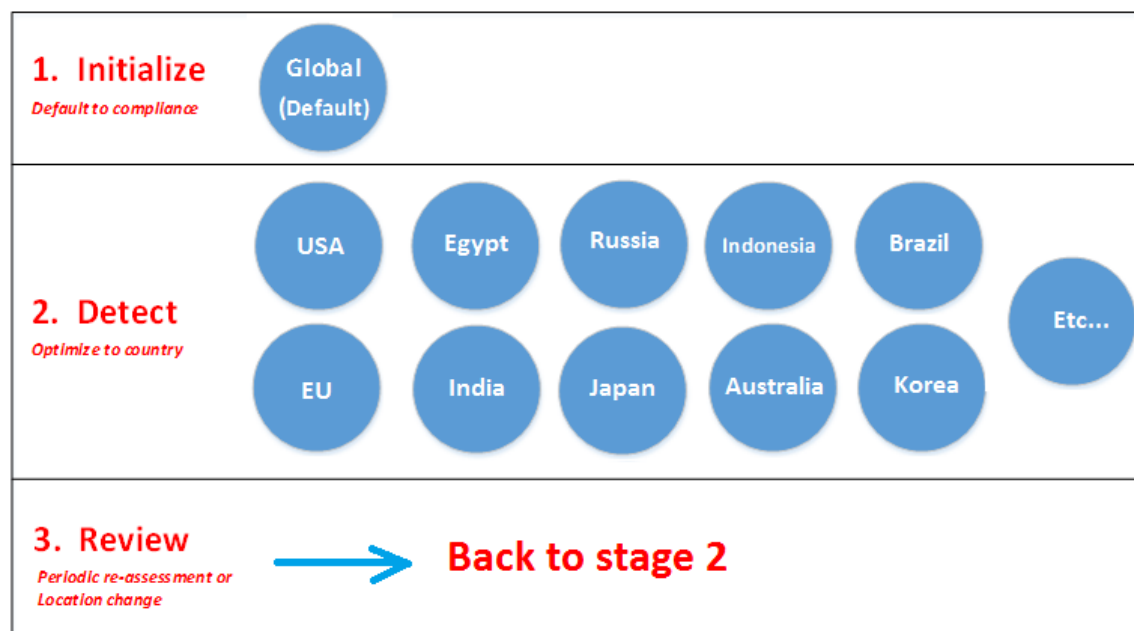
The DRS provides a significant improvement in compliance reliability by ensuring the compliance always aligns to the adapter's location. It also provides the ability to react more quickly to changing regulations that can be applied precisely to the relevant country or countries without impacting optimizations to any other country.

8.2 Operation

DRS utilizes a proprietary country detection mechanism that, through a combination of field surveys and theoretical analysis, demonstrated >99.9999% accuracy. DRS's basic operational flow consists of initializing the adapter to a most-of-world (MoW) or "Default" configuration, detecting and optimizing to a specific country, and using a feedback loop to periodically review the location and change the configuration as necessary. This operational flow is designed to ensure an optimized environment of regulatory compliance and user experience:

- 1) **Initialize:** Configure the adapter to MoW compliance by using minimum channel configurations to meet both FCC and ETSI regulations. This MoW configuration is used to ensure a good user experience.
- 9) **Detect:** Utilizing the proprietary country detection mechanism, configure to an optimized channel map for the given country detected. In most cases, the adapter will optimize around FCC regulations or ETSI regulations. In exceptions, the adapter will disable channels (for example, Indonesia), channel widths for 802.11ac (such as Russia before its adoption in 2016), or bands (such as Tunisia). When no country is detected, the adapter will remain in the "Default" configuration. Country maps and channel configurations are detailed in the subsequent section.
- 10) **Review:** Periodically reassess the location to ensure the configuration is valid or determine that it should change. The reviews are triggered under any condition that indicates a user has changed location. Since Wi-Fi is a local-area networking technology, this can be achieved by using network connectivity changes (system power on/resume, profile change, airplane mode, etc.) to trigger the review. DRS also uses a 1 hour timer to reassess the location and ensure continual monitoring.

Figure 8–1 DRS flow



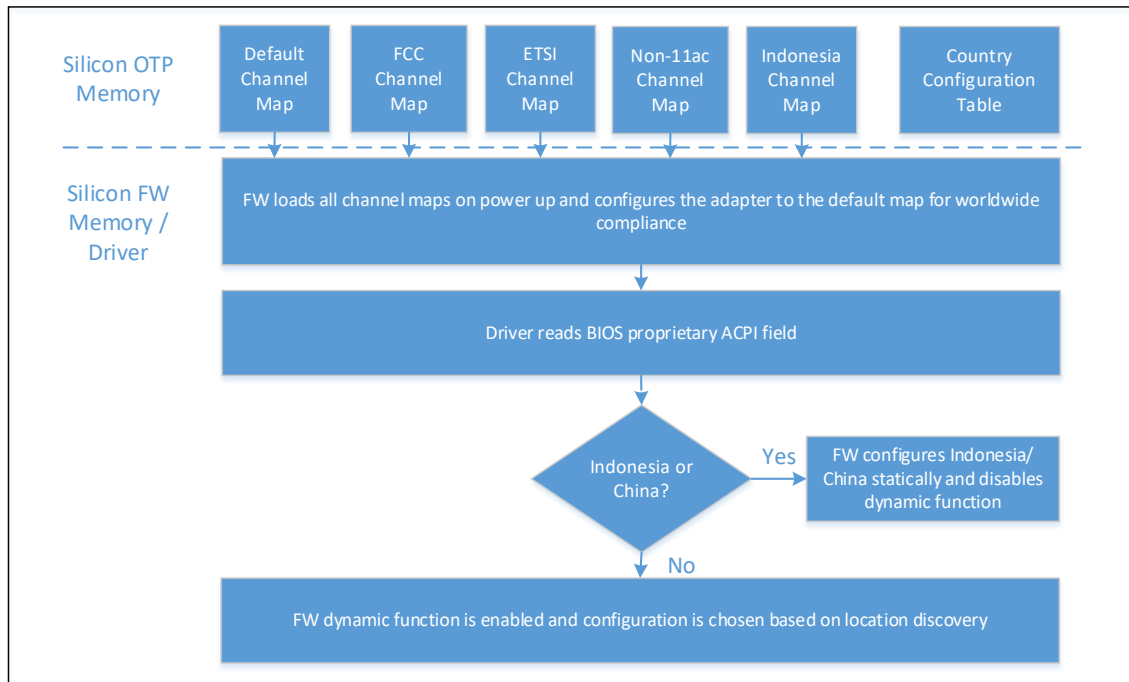
In addition to the operational flow described, a regulatory exception exists where

- (1) There are significant channel restrictions from the MoW configuration, and
- (2) System (platform) approvals are required that place the regulatory responsibility on OEMs

In this case (and for any future scenarios that may require this capability), DRS provides the ability to configure the adapter, at the system level, to a static channel map that complies with the specific country restrictions (example is Indonesia restrictions). The system (platform) configuration is done by indication that specify the specific country target through a custom BIOS ACPI setting. Please refer to Section 8.6 for details on programming the BIOS. for example, when the BIOS is configured to Indonesia, the device driver is designed to read this setting, disable the dynamic location detection mechanism, and statically configure the adapter to the Indonesia channel map.

8.3 DRS architecture

The DRS architecture, including the optional BIOS configuration, is shown in Figure 8–2. DRS leverages multiple product components.

**Figure 8–2 Dynamic regulatory architecture**

8.3.1 Regulatory Tx values tables

The device contains four full Tx channel maps:

- Table 0 – default table that is used before country location is confirmed. It represents the minimum values of the other tables.
- Table 1 – US FCC and alike
- Table 2 – ETSI Limits and alike
- Table 3 – contains Other remaining Tx Power limitations

8.3.2 Country profiles

The device supports up to 31 country profiles. Each profile defines which Tx power table to use per sub-band.

8.3.3 Mapping country code to country profile

The device contains a table mapping country code (total of 129) to the relevant profile.

8.3.4 Determining the location

Intel Wi-Fi driver and firmware executes a proprietary mechanism to determine the location. Based on the location found, the FW chooses the country profile based on the table mapping country code to profile.

If the platform BIOS is configured to a regulatory static configuration, the driver and firmware set the location accordingly, and disable the location detection mechanism.



8.4 Validation of regulatory compliance

Intel owns the validation of the DRS feature. This includes validation of the location detection mechanism, choosing the correct country profile, and enabling/disabling allowed/not-allowed channels and bandwidth.

8.5 Performance testing

When the adapter cannot determine the regulatory domain, it will default to the global “Default” profile. This can result in lower TX performance than the maximum the adapter is capable of. If performance testing with other profiles is desired, the customer is encouraged to

1. Order a limited number of adapters hard coded to other domain profiles (such as FCC). Please contact your Wireless TAM for availability.
2. Use the ANT tool and force regulatory domain for testing performance. The ANT tool uses a command line function to set DRS’s MCC (Mobile Country Code) to a specific country configuration. It runs over the standard driver to ensure the adapter’s production configuration is tested. Details are included in the tool’s user guide. Please note that this configuration is time-limited and the device will disconnect after the timer expires, to prevent bypassing the DRS mechanism.
3. For PHY parameters tests (Tx power, EVM), the customer can use the DRTU tool. The DRTU tool supports configuration to a specific country code.

8.6 BIOS configuration

The device supports BIOS configuration to support regulatory special cases, as follows:

1. Static regulatory setting – Set to a specific country and disable the dynamic regulatory scan
2. Static SAR tables to configure the platform to have specific SAR limits (per antenna, per sub-band)
3. Dynamic SAR tables – Choose the SAR limits based on platform triggers (requires application that support this mode)

For additional information on updated BIOS configuration, please refer to the BIOS guidelines doc.

**Figure 8–3 Regulatory domain (WRDD) object definition**

```
Name (WRDD, Package())
{
    // Field Name          Field Type
    Revision,              // DWordConst

    Package()              // Default Configuration
    {
        DomainType,        // WiFi = 0x7
        RegulatoryDomain,   // Country identifier as defined in ISO/IEC 3166-1
                           // Default(AP)=0x4150, China(CN)=0x434E
    },
}) // End of WRDD object
```

Table 8–1 WRDD field descriptions

Field	Format	Description
Revision	DWordConst	Revision identifier for this structure. Set to 0 always.
DomainType	DWordConst	Identifies the domain this object is providing default configuration data for. The domain type identifies a bitmap-based value, so that default values for a combination of domains can be specified. Use 0x7 for Wi-Fi in this instance.
RegulatoryDomain	WordConst	Defines the regulatory domain to be used: Default(AP) = 0x4150 // Device ignores and resumes dynamic operation China(CN) = 0x434E // Device configures statically to China

Additional details, including a sample configuration, can be found in the BIOS reference spec:

Platform Reference Code for 5th Generation Intel® Core™ Processor Platforms (codenamed Broadwell)

The WRDD object is referenced in the following locations within the spec:

BroadwellRcPkg\AcpiTables\Dsd\GlobINvs.asl

BroadwellRcPkg\Cpu\SampleCode\Include\Protocol\GlobalNvsArea.h

BroadwellRcPkg\AcpiTables\SampleCode\AcpiPlatform\Dxe\AcpiPlatform.c

BroadwellRcPkg\AcpiTables\SampleCode\Library\PlatformAcpiLib\AcpiGnvsInitLib.c

Note: There are two instances of the WRDD object in the reference spec. Only the first instance needs to be created in this scenario.





9 Platform Design Guidelines

This section includes important platform design and implementation aspects that the OEM should take into consideration when implementing a platform that would accommodate this product. Jefferson Peak is an integrated connectivity RF companion module, and there has special platform design guidelines are different from standard M.2 connectivity design features.

Besides having new interface requirements, integrated connectivity allows designing the platform so as to support both integrated and discrete connectivity M.2 modules using a single platform design. This allows the OEM to have one motherboard design accommodating either a Companion RF module or a discrete M.2 card which can be “swappable” on the same M.2 socket.

This section focuses on the dual CNVi/Discrete design, and therefore will include guidelines applicable to the Jefferson peak M.2 card as well as to other discrete M.2 cards.

9.1 Socket 1 key options for 2230 cards

Socket 1 has two options: Key E and Key A. Each key with different supported list of I/Fs as defined in the M.2 specification.

In general the different keys should be used in the following cases:

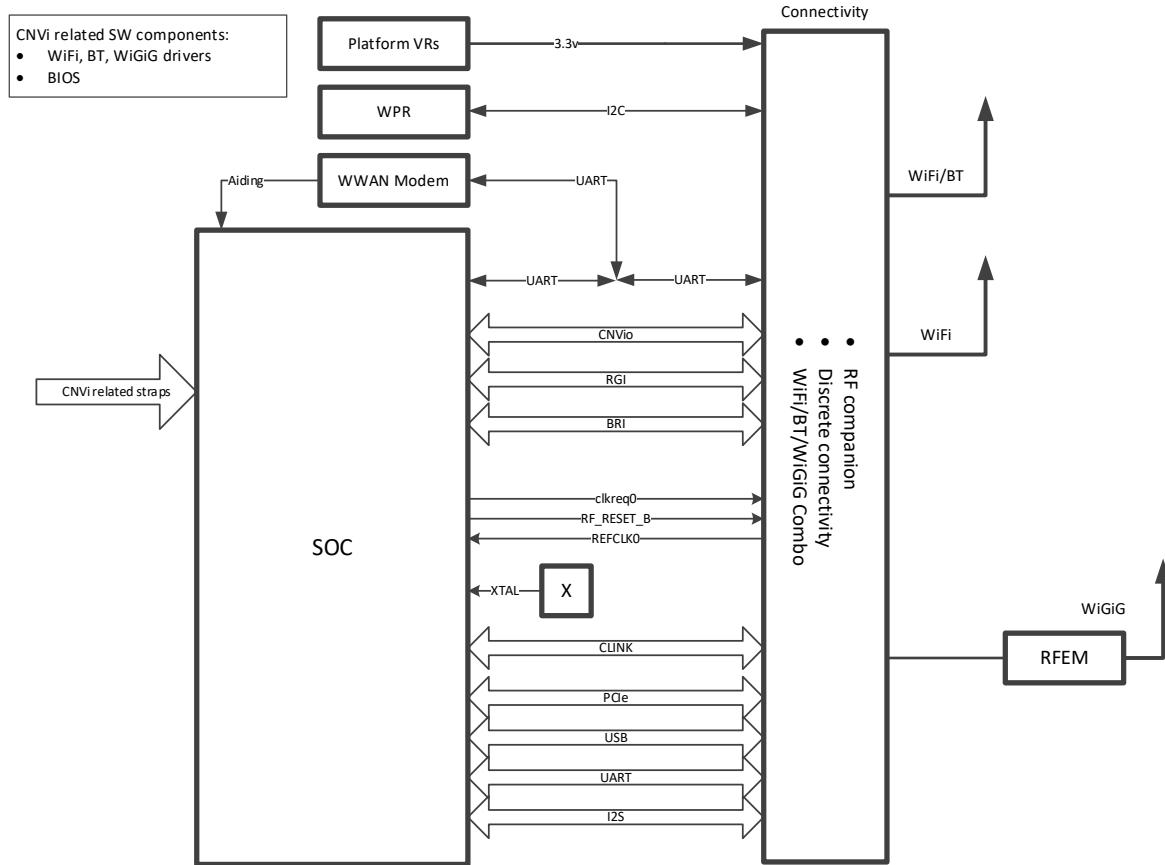
- **Key E:** When UART/I2S for Bluetooth® is required
- **Key A:** When WiGig with display port is required – N/A for 2017 products
- **Hybrid Key E:** When CNVi should be supported and when swappable CNVi/discrete should be supported

In order to support the Jefferson Peak, or any other CNVi RF companion module the third option shall be used on the design. The Hybrid Key E can be designed in a few different variants allowing some level of flexibility including:

- Supporting integrated connectivity (CNVi) only
- Supporting swappable integrated/discrete connectivity (CNVi)

9.1.1 Socket 1 Hybrid Key E scheme

The high level block diagram in Figure 9–1 shows the platform-level view of CNVi, including all related system components. Note that the connectivity block represents a few alternative options: Companion RF, Discrete, and Wi-Fi/ Bluetooth®/WiGig Combo, all of which can be used in the design but are mutually exclusive (only one can exist at a specific time).

Figure 9–1 Platform connections to CNVi – Hybrid Key E scheme


9.1.2 Connectorized Hybrid Key E (2230) pin-out

The M.2 socket with the Hybrid Key E scheme is intended to be used with a proprietary pinout. This scheme is called “Hybrid Key E” due to the mechanical similarity to a Key E connector and the ability to support both Companion RF and discrete modules. When designing a motherboard with this scheme, one can have the same M.2 socket supporting three (3) different connectivity cards:

- (1) CNVi Companion RF module (CRF)
- (2) Standard M.2 discrete module (Discrete), and
- (3) WiGiG/Wi-Fi combo module (Combo) – N/A for 2017 products

The ability to swap between these three cards on the same M.2 socket while using the same motherboard design is an important feature desired by PC platform OEMs.



Platform Design Guidelines

When designing the motherboard M.2 socket and routing according the Hybrid Key E scheme, and subject to certain assumptions that will be defined later, the following basic properties are guaranteed:

- Inserting any one of the three optional cards (Namely CRF, Discrete and Combo) to the M.2 socket will be safe (meaning no damage to the motherboard or card will occur).
- All three options can be used and will function as desired, subject to the following:
 - For CNVi: No restrictions apply
 - For Discrete: The most commonly used interfaces will work. Some interfaces will not be available and therefore some operation modes will not function. A list of restrictions on modes and interfaces can be found in Table 9–1.

The pinout for the Hybrid Key E socket on the motherboard is shown in Figure 9–2. The inner columns show the Companion RF proprietary signals at their assigned pins. The Companion RF signals, listed with the prefix “/,” signify that they are electrically MUX’d inside the PCH/SoC and are shared. Due to this internal SoC sharing, these signals do not require any jumpers to select between the two functions. Note that there are six (6) such signals.

Figure 9–2 2230 Hybrid Key E socket pinout (names refer to platform socket side)

	Standard M.2 Key E	LcP Signals	LcP Signals	Standard M.2 Key E	
74	+V3P3A		GND		75
72	+V3P3A		WT_CLKP	REFCLKN1	73
70	PEWake1# (IO)(0/3.3V)		WT_CLKN	REFCLKP1	71
68	CLKREQ1# (IO)(0/3.3V)				69
66	PERST1# (O)(0/3.3V)		WT_D0P	PERn1	67
64	RESERVED	REFCLK0 (I)(1V@38.4MHz)	WT_D0N	PERp1	65
62	ALERT# (I)(0/1.8V)	A4WP_IRQ#			63
60	I2C_CLK (O)(0/1.8V)	A4WP_I2C_CLK	WT_D1P	PETn1	61
58	I2C_DATA (IO)(0/1.8V)	A4WP_I2C_DATA	WT_D1N	PETp1	59
56	W_DISABLE1# (O)(0/3.3V)				57
54	W_DISABLE2# (O)(0/3.3V)				55
52	PERST0# (O)(0/3.3V)				53
50	SUSCLK(32kHz) (O)(0/3.3V)	C_P32K (3.3V Tolerant)			51
48	COEX_TXD (O)(0/1.8V)				49
46	COEX_RXD (O)(0/1.8V)				47
44	COEX3 (IO)(0/1.8V)				45
42	CLink CLK				43
40	CLink DATA				41
38	CLink RESET (O)(0/3.3V)				39
36	LPSS UART RTS (O)(0/1.8V) / BRI_DT (MUX'd in PCH/SoC)				37
34	LPSS UART CTS (I)(0/1.8V) / RGI_RSP (MUX'd in PCH/SoC)				35
32	LPSS UART Tx (O)(0/1.8V) / RGI_DT (MUX'd in PCH/SoC)				33
E	Connector Key		Connector Key		E
	Connector Key		Connector Key		
	Connector Key		Connector Key		
	Connector Key		Connector Key		
22	LPSS UART Rx (I)(0/1.8V) / BRI_RSP (MUX'd in PCH/SoC)		WGR_CLKP	SDIO Reset#(O)(0/1.8V)	23
20	UART Wake# (I)(0/3.3V)		WGR_CLKN	SDIO Wake#(I)(0/1.8V)	21
18	GND	GND/LNA_EN (LcP Production)			19
16	LED2# (I)(OD)		WGR_D0P	SDIO DAT3(IO)(0/1.8V)	17
14	PCM_OUT (O)(0/1.8V) / CLKREQ0 (MUX'd in PCH/SoC)		WGR_D0N	SDIO DAT2(IO)(0/1.8V)	15
12	PCM_IN (I)(0/1.8V)				13
10	PCM_SYNC (O)(0/1.8V) / RF_RESET_B (MUX'd in PCH/SoC)		WGR_D1P	SDIO DAT1(IO)(0/1.8V)	11
8	PCM_CLK (O)(0/1.8V)		WGR_D1N	SDIO CMD(IO)(0/1.8V)	9
6	LED1# (I)(OD)				7
4	+V3P3A				5
2	+V3P3A				3
					1



9.1.3 Special considerations for the Hybrid Key E scheme

The Hybrid Key E scheme relies on assigning multiple functions to M.2 connector pins and to PCH pins. This causes a significant reduction of the amount of signals that needs to be routed between the SoC and the M.2 Module at the expense of additional dependency between modes, and the loss of some functionality. The different dependencies between multiple functions pins and M.2 card functionality is described in the following section.

9.1.3.1 Shared M.2 socket pins

The following M.2 pins are shared between different functions:

V3P3A, GND

This is the M.2 card power supply (3.3V) and Ground pins, respectively. Both have multiple pins on the connector. These pins have the same purpose in either discrete or CNVi implementations, and therefore are not affected by the Hybrid Key E scheme.

PCIe-1/CNVio

These are six pins that are assigned to the PCIe-1 bus in the M.2 standard pinout. This bus has three differential pairs, two for the PCIe* data lanes (one per direction) and one for the PCIe* clock. In the Hybrid Key E scheme, these signals are used for the CNVio interface from Pulsar to the companion RF chip. Due to this sharing, the Hybrid Key E scheme does not support PCIe-1.

SDIO/CNVio

These are eight pins that are assigned to the SDIO bus in the M.2 standard pinout. This bus has eight signals, four bi-directional for the SDIO data, one bi-directional command signal, one clock (SoC to M.2) and two control (Reset SoC to M.2, Wake M.2 to SoC). In the Hybrid Key E scheme these signals are used for CNVio interface the RF companion chip to Pulsar (six for CNVio and two for ground). Due to this sharing, the Hybrid Key E scheme does not support SDIO.

PCM/ClockReq and Reset

The standard M.2 defines four pins for a dedicated PCM audio serial bus. In the Hybrid Key E scheme, two of these signals are used for CNVi Clock (from RF companion to SoC) and Reset (For SoC to RF companion). Since the PCM serial bus is connected to PCH GPIO pins, and the CNVi clock request and reset pins are also connected to PCH GPIO pins, it is possible to have support for both PCM bus and CNVi signals by changing the PCH GPIO muxing function select. Due to this sharing, the Hybrid Key E scheme can still support PCM (for discrete connectivity with PCM support).

UART (Bluetooth®) / BRI and RGI

The standard M.2 defines four pins for a dedicated UART serial bus for Bluetooth®. In the Hybrid Key E scheme, all these signals are used for CNVi BRI (Bluetooth® radio interface) and RGI (radio generic interface), each comprised of two signals (one per direction). Since the UART serial bus is connected to PCH GPIO pins, and the CNVi BRI and RGI are also connected to PCH GPIO pins, it is possible to have support for both the UART bus and CNVi signals by changing the PCH GPIO muxing function. Due to this sharing, the Hybrid Key E scheme can still support Bluetooth® UART (for discrete connectivity with BT-UART support).

SUSCLK/P 32K

These signals are both functionally similar. In the M.2 standard, this pin is optionally connected to a 32KHz RTC clock. This pin is not used by JfP2.

GND/LNA EN

This signal is used for different purposes in CNVi and discrete, but in both cases should be connected to ground; therefore, it does not affect functionality.



NFC I/F, and A4WP+Ref clock

In the Hybrid Key E scheme, only the REFCLK0 signal is used. This REFCLK0 signal connects the reference clock (single ended, 1V p-p, 38.4MHz) from the RF companion to the SoC. The remaining three signals are not used.

9.1.3.2 Non-shared M.2 socket pins

Some pins on the M.2 connector are not shared, meaning they are not used for any CNVi function. The functions of these pins can still be impacted by the Hybrid key E scheme as will be described here.

PEWake1#, CLKREQ1#, PERST1#

These are three control signals used by the PCIe-1 bus in standard M.2 cards. Although these signals are not shared with any other function, they have no usage in a Hybrid Key E scheme design. This is because the PCIe-1 bus by itself is not usable. (See “PCIe-1/CNVio,” above.)

PCIe-0 Bus

This consists of six signals (three differential pairs) used for PCIe* data to and from the SoC, and a single pair used for the PCIe* bus clock. In a CNVi RF companion, these signals are left unused. In a discrete module, these signals are being used as the Wi-Fi bus interface.

W_DISABLE1#, W_DISABLE2#

These are used for Wi-Fi and Bluetooth® RF-KILL control, respectively. (Asserting these signals shuts off the RF transmission or the relevant core.) The functions of these signals are the same for Hybrid Key E, and therefore they are not affected by this scheme.

PEWake0#, CLKREQ0#, PERST0#

These are three control signals used by the PCIe-0 bus in standard M.2 cards. They should be routed to SoC pins that are assigned to GPIOs in Discrete or Combo modes.

Coex UART interface

This interface consists of three signals (two UART bus signals and one GPIO). They are used for Wi-Fi/ Bluetooth®-LTE coexistence signaling in the M.2 standard definition. Since these pins are left unused in the RF companion, they can still be used with a discrete M.2 card even when designing with the Hybrid Key E scheme. In platforms that are designed to support a WWAN modem and Hybrid Key E, there should be three pins connected to each signal, to allow the modem to connect to the M.2 pin (in the discrete connectivity case) or to the PCH (in the CNVi case).

CLINK interface

This interface consists of three signals (clock, data and reset). This bus is an Intel-proprietary bus. Since these pins are left unused in the RF companion, they can still be used with a discrete M.2 card, even when designing with the Hybrid Key E scheme.

LED1, LED2

These are optional pins that are assigned to drive LEDs on the platform in the standard M.2 cards. They are used for the same function when using CNVi, and therefore are not affected by the Hybrid Key E scheme.

USB bus

The standard M.2 defines two pins for a differential USB bus. This bus has no usage in the RF companion. When using a standard M.2 discrete card, the pins will have the standard functionality and are not affected by the Hybrid Key E scheme.

The different connectivity interfaces as used by a discrete connectivity (Standard M.2, Intel connectivity, or TPV) and CNVi RF companion card are summarized in Table 9–1. The table also points to the different restrictions posed by the use of a Hybrid Key E socket design on the motherboard.

**Table 9–1 Hybrid Key E interface mapping for different connectivity cards**

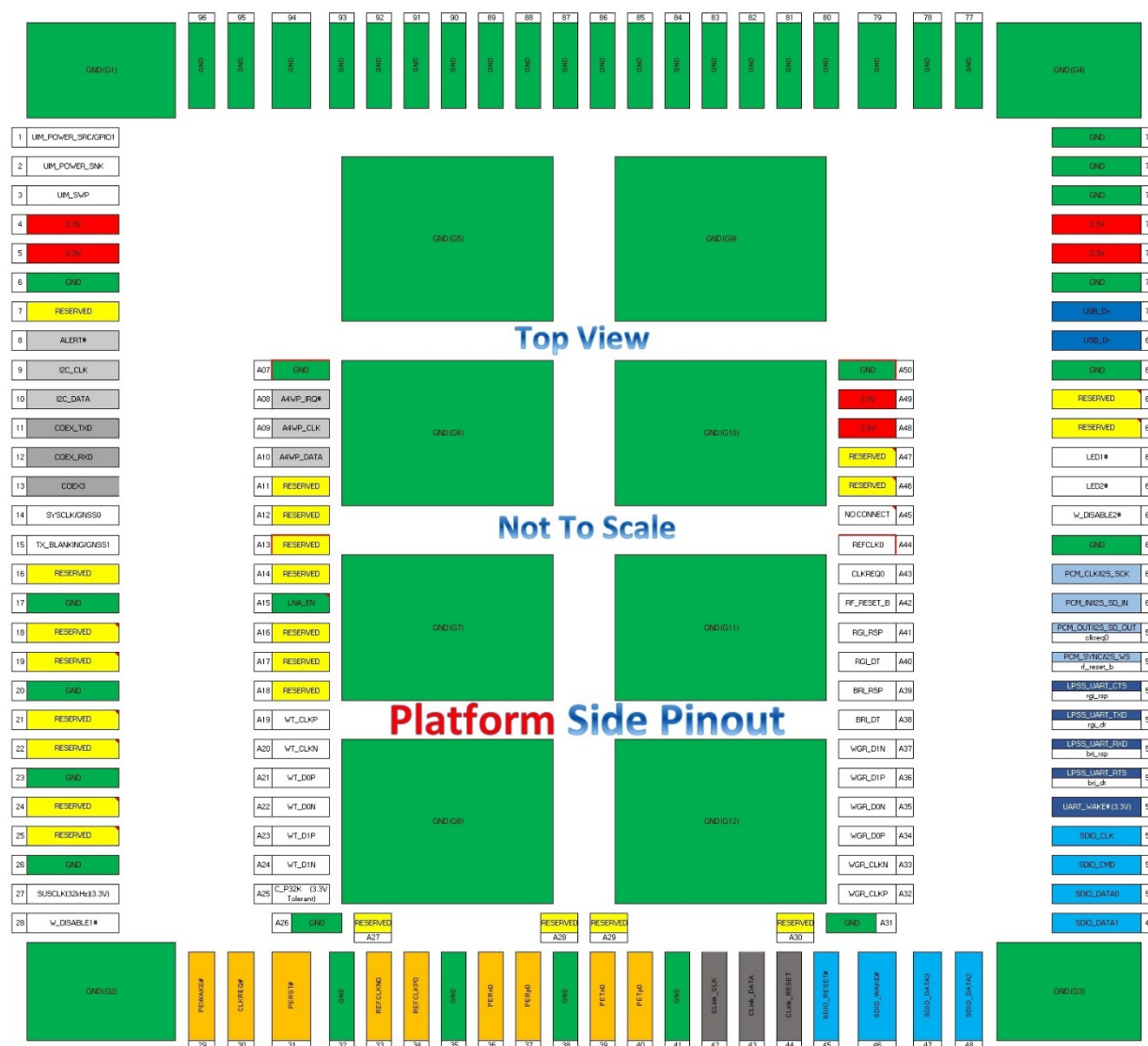
M.2 Interface	CNVi	Discrete
PCIe-1	M.2 pins are not connected to the CRF. Wi-Fi uses internal IOSF to interface the host.	Used for Wi-Fi host interface
PCIe-2	Not functional Pins are connected to CRF and Pulsar CNVio and can't be used as PCIe*.	Not functional Pins are connected to Pulsar CNVio and can't be used as PCIe*.
Wi-Fi SDIO	Not functional Pins are connected to CRF and Pulsar CNVio and can't be used as SDIO.	Not functional Pins are connected to Pulsar CNVio and can't be used as SDIO.
Wi-Fi CLINK	M.2 pins are not connected to the CRF. Wi-Fi uses internal CLINK to interface the ME.	Used for Wi-Fi CSME interface
Wi-Fi RF-KILL	Used (optional)	Used (optional)
Bluetooth® USB	M.2 pins are not connected to the CRF. Bluetooth® uses internal U2U to interface the host.	Used for Bluetooth® USB interface
Bluetooth® UART	M.2 pins are not connected to the CRF. Bluetooth® uses internal UART to interface the host.	Used for Bluetooth® UART interface
Bluetooth® I2S (Audio)	M.2 pins are not connected to the CRF. Bluetooth® uses internal I2S to interface the host.	Used for Bluetooth® I2S interface
Bluetooth® wake	M.2 pin is not connected to the CRF. Bluetooth® uses internal vGPIO.	Used for Bluetooth® wake signal
Bluetooth® RF-KILL	Used (optional)	Used (optional)
NFC	Not functional Pins are connected to A4WP bus and to Refclock (38.4M system clock) and can't be used for NFC.	Not functional Pins are connected to A4WP bus and to Refclock (38.4M system clock) and can't be used for NFC.
I2C bus to A4WP	Used for A4WP support to connect to platform WPR module.	Used for A4WP support to connect to platform WPR module.
3.3V Power supply pins	Used per M.2 standard	Used per M.2 standard
GND	Used per M.2 standard	Used per M.2 standard

9.1.4 Soldered-down (1216) pin-out

The RF Companion SD-1216 module has the same mechanical outline as the standard M.2 connectivity type 1216-S3. The standard M.2 land pattern is modified to accommodate the proprietary the RF companion module signals. Instead, it has an additional set of solder pads which don't overlap with the standard solder pads. This allows having a single motherboard design that can accommodate either a standard M.2 1216 card or an RF companion 1216 card. However, unlike in the connectorized case, swapping cards requires removing a soldered-down module, and so can't be done with a simple socket card exchange. Additionally, the assembly tooling and BOM should change between a discrete and CNVi motherboard assembly.

The special pad-out required for supporting CNVi and discrete is shown in Figure 9–3.

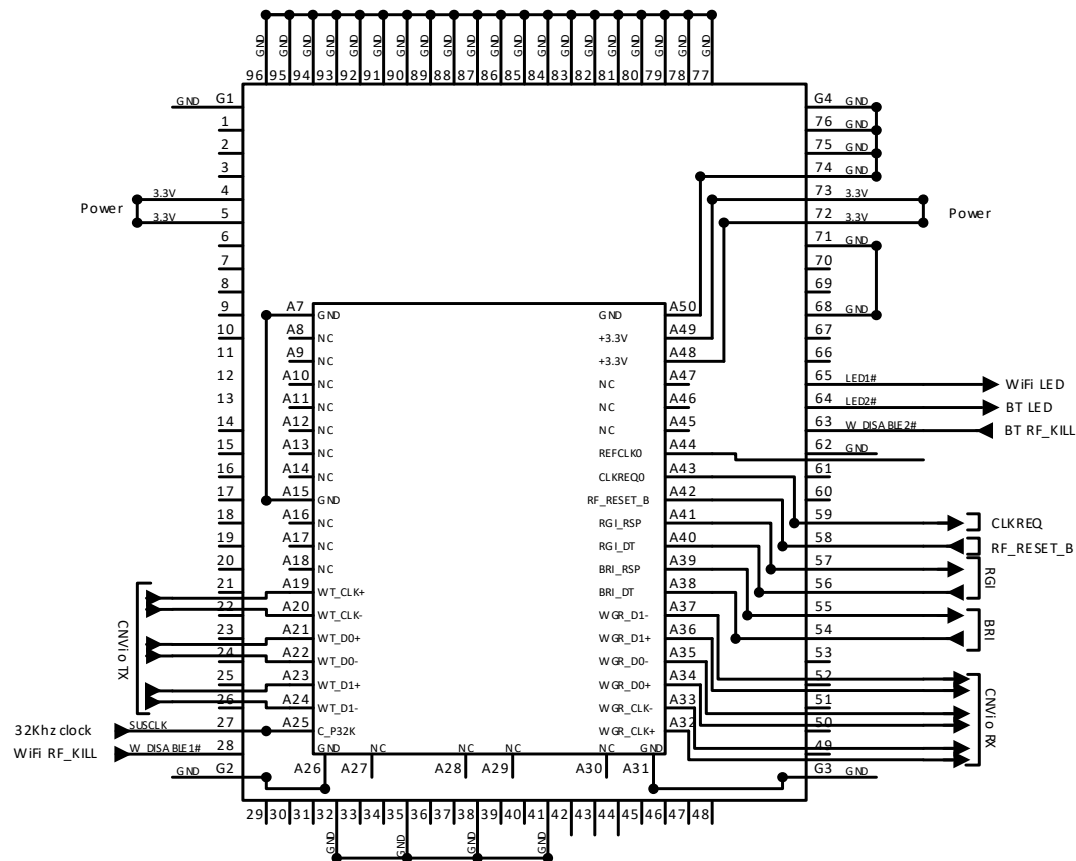
Figure 9–3 SD-1216 module pad-out for supporting CNVi and Discrete 1216 modules



9.1.5 Breakout example for JfP soldered-down module

The soldered-down JfP module has a special pad shape, which combines the standard M.2 pad ring on the outside with the new inner ring of the CNVi pads. It is recommended that the OEM consider all signal properties when designing the motherboard for dual discrete/CNVi design supporting Jefferson Peak 1216. An example for the breakout layout for a type-3 board (with no micro-via) is shown in Figure 9–4. Note that in order to keep the picture clear, this example shows only two signal layers (top layer and third layer) while the other layers are not shown. Also there is an assumption that the second layer shall be ground.

Figure 9–4 Board layout example showing breakout from JfP 1216 pads (design for CNVi only)



The diagram illustrates the pin-to-pin connections between the Raspberry Pi 400 (left) and the Raspberry Pi 4 Model B (right). The connections are organized into two main sections: one for the Raspberry Pi 400 pins (left) and one for the Raspberry Pi 4 Model B pins (right).

Power and Coex signals:

- Power: 3.3V and GND connections.
- Coex signals: COEX_TXD, COEX_RXD, COEX3.

CNV io TX and 32Khz clock:

- CNV io TX: Connections for CNV io TX signals.
- 32Khz clock: Connection for the 32Khz clock signal.
- Wifi RF_KILL: Connection for the Wifi RF_KILL signal.

Peripheral signals:

- BT USB: Connections for BT USB signals.
- Wifi LED: Connection for the Wifi LED signal.
- BT LED: Connection for the BT LED signal.
- BT RF_KILL: Connection for the BT RF_KILL signal.
- REFCLK 38.4Mhz: Connection for the REFCLK 38.4Mhz signal.
- I2S: Connections for I2S signals.
- CLKREQ: Connection for the CLKREQ signal.
- RF_RESET_B: Connection for the RF_RESET_B signal.
- UART: Connections for UART signals.
- GPIO: Connections for GPIO signals.
- CNV io RX: Connections for CNV io RX signals.

The diagram shows a complex interconnection of signals, with many pins connected to GND or VCC. The connections are organized into two main sections: one for the Raspberry Pi 400 pins (left) and one for the Raspberry Pi 4 Model B pins (right).

- The OEM should make sure to follow the M.2 definitions of signal names and directions (I/O TX/Rx etc.) and avoid confusion between platform side and device side.
- Note that some lines are bidirectional, such as PCIe* CLKREQ, PEWAKE.

The OEM should apply pullups and pulldowns in the platform side according to Table 9-2.

I/F	Signals	PU/PD Guideline	Rationale
BRI/RGI Bluetooth® UART	BRI_DT / RTS	None	Intel SoC with CNVi support have internal PU/PD as needed.
	RGI_RSP / CTS	PU	Intel SoC with CNVi support have internal PU/PD as needed.



I/F	Signals	PU/PD Guideline	Rationale
	BRI_RSP / Rx	PU	Intel SoC with CNVi support have internal PU/PD as needed.
	RGI_DT / Tx	PU	Intel SoC with CNVi support have internal PU/PD as needed.
Bluetooth® UART	WAKE#	PU	Open drain, required by M.2
W_Disable#		PU	Required by Intel platform design guidelines. This signal has an internal pull-up tied to 1.8V
PCIe*	PEWAKE#	PU	Open drain, required by M.2
	CLKREQ#	PU	Open drain, required by M.2
	PERST#	PD	Required by Intel platform design guidelines
	Other PCIe* signals	None	PCIe* spec
38.4 Ref clock	RefCLK	PD	

The OEM must avoid using PU/PD when not needed or when required not to be used. If this rule is not followed, it will result in a back-bias condition, where the IO is getting voltage before the device side is ready for it.

9.1.8 IO connection scenarios and best practices

The motherboard designer should address the following requirements for the sake of avoiding failsafe problems, reducing unneeded leakage, and for following best-practice design rules:

- Level-shifter back-bias prevention
 - Level shifter shall not set value in A side when not getting voltage in B side.
 - Rationale:** Prevent back-bias and wrong logic conditions.
 - Level shifters shall be back-bias protected.
 - Rationale:** The level shifter is often supplied with a different supply than the IO connected to it. During ramp up/down states there might be a back-bias scenario.

9.1.9 I/F specific guidelines

9.1.9.1 CNVio signals

The CNVio signals connect the RF companion module and the SoC. They are used as the main data bus for Wi-Fi to transfer data between the Pulsar and the RF companion chip. The CNVio signals are physically similar to the MiPi DPHY standard, but have a different (and Intel-proprietary) protocol.

Since the physical layer of the CNVio is similar to a standard, the user should follow the MiPi DPHY routing signal requirements. These are well documented in the MiPi DPHY standard specification. (See Chapter 7 of the MiPi DPHY standard: "Interconnect and Lane Configuration.")

The CNVio bus is source-synchronous, running at up to 1280Mbps. Each lane has data carried over a differential pair, and each direction may have multiple lanes and a single clock, driven by the source.

Routing

The routes of the two traces of each lane must match as much as possible. Moreover, since the CNVio uses one clock signal for multiple lanes in each direction, there should also be good delay matching



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between the two data lanes and the clock. There are no special delay-matching requirements between lanes in opposite directions.

Table 9–3 CNVio recommended parameters

Parameter	Value	Comment
Differential pair length matching:	0.02UI For 1280M: <80 mil	This parameters may effect EMI and RFI
Characteristic impedance	85 ohm differential	50 ohm to ground for each trace
Maximum length	10 inch	9 inch from M.2 connector pins to SoC pins
Maximum resistance	5 ohm	50 ohm to ground for each trace
Shielding	Berried microstrip (Stripline)	Recommended for minimizing EMI/RFI
Delay matching between pairs of the same direction	Better than 80 mil	Including the 2 lanes and the clock in every direction
Vias	Minimize usage	Recommended to avoid Via connections as much as possible and follow differential
BER	1E-12	Standard PHY bit error rate for a CNVio lane

9.1.9.2 RGI and BRI signals

These are GPIO signals (1.8V) running between the SoC and the RF companion module. The BRI and RGI signals share the same traces as UART signals (for discrete). Since the UART baud rate is expected to be lower than the BRI/RGI toggle rate, it can be assumed that the BRI/RGI sets the requirements for this bus. BRI and RGI are two bi-directional busses. No special control impedance is needed. The BRI and RGI packets are protected by error-correction coding and with standard routing and signal integrity practices applied, no errors are expected to be noticed on the busses.

9.1.9.3 38.4M reference clock signal

Ref Clock is a 38.4M clock signal which is generated by the RF companion module and sent to the SoC. This clock can be used as the SoC main clock (in clock sharing configuration) or as the Pulsar clock (in non-clock sharing configuration). When using the latter option, the SoC should have another clock for its operation, but Pulsar (within the SoC) will always get the 38.4M clock coming from the Companion RF module.

It is recommended to route the clock with special care while maintaining clock routing practices, preferably as a microstrip, to minimize EMI/RFI and susceptibility to noise.

Please refer to TA #574558 for more information on how to reduce the ESD risk related to the JfP 38.4MHz CLK signal.

See Table 9–4 for 38.4MHz clock characteristics.

Table 9–4 38.4MHz clock signal characteristics

Parameter	Units	Min	Typ	Max	Notes
Output Clock Frequency	MHz		38.4		
Trace Length to Drive	Inches	1	5	10	
Trace Characteristic Impedance to Drive	Ohm	30	50	75	



Parameter	Units	Min	Typ	Max	Notes
Load Resistance (RL) to Drive	KOhm	8	10		
Load Capacitance (CL) to Drive	pF	10	20	35	Includes PCB Trace + SoC input capacitance
Output High Voltage	V	0.9	1	1.15	
Output Low Voltage	V	-0.15	0	0.15	
Output Clock Rise/Fall Time	ns	1	3	5	Measured at 20%–80%
Output Clock Duty Cycle	%	45		55	Measured at 50% crossing

9.1.9.4 Wi-Fi/Bluetooth®/LTE coexistence signals

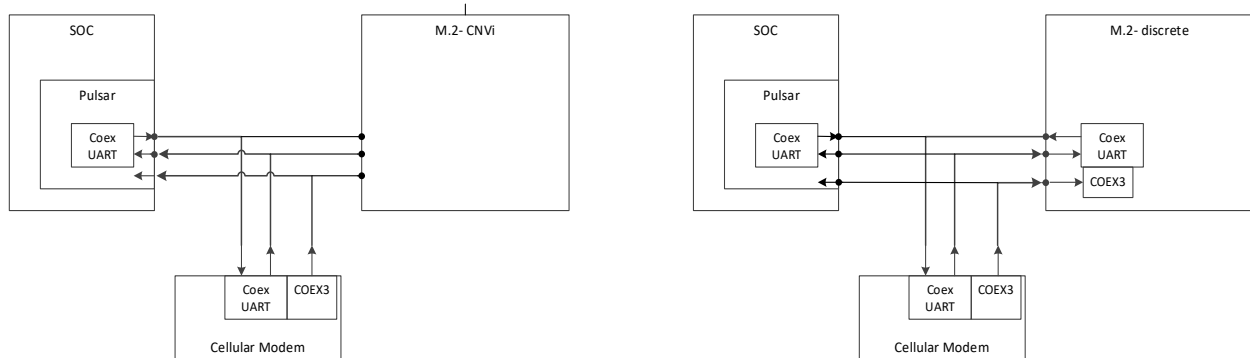
In order to allow a Hybrid Key E scheme supporting both connectivity and a cellular modem, there is a need to connect the modem coexistence bus in a configuration that will allow the modem to connect to the connectivity coexistence control logic. In Intel connectivity modules, this logic may reside in the M.2 module or in the SoC, depending on whether the CNVi or discrete solutions are used:

- For CNVi, the logic that is connected to the coexistence bus resides in Pulsar, which is part of the SoC.
- For discrete M.2 cards, this logic resides in the module.

As a result, when a motherboard design contains a modem, and it is desired that it be able to support CNVi and discrete on the same M.2 socket, there is a need to have a 3-way connection of the board, as shown in Figure 9–6. In this diagram, the red lines represent lines that are unused in each connection scenario. One can simplify the routing by adding a jumper resistor to select between the two configurations; however, this will result in losing the option to swap between CNVi and Discrete on the board. Any such swapping will then require a board hardware change for changing the jumper resistor position.

Note that when doing this 3-way connection between SoC, M.2 and the modem, there will always be an unused signal that is not optimally terminated for that connection. This signal is shown in red in the connection diagram. The effect of this signal is similar to a stub that adds undesired impedance change to the trace. The effect of this stub on the UART bus depends on several system parameters: distance between the different UART pins, UART bus speed, and electrical characteristics of the UART drivers and receivers (referenced to the signal pins). This effect must be considered and analyzed through design practices or simulations to ensure that signal integrity is not compromised. For this analysis, the UART baud rate shall be assumed to not be higher than 4Mbaud.

Figure 9–6 Coexistence UART for connectivity/modem 3-way configuration





9.1.10 Connectivity module power control

The connectivity module power supply pins shall be connected directly to the rail DSW.

To ensure proper operation of the integrated connectivity module, the use of a power switch to control the M.2 module power shall be avoided. The Jefferson Peak module is not compatible with the SLP_WLAN control signal. Note that the Jefferson Peak module was designed with low-leakage power, and therefore does not require any external power control to be used during normal operation.

9.1.11 Power supply de-coupling

It is required to have decoupling caps on the power feeds in each end of the connector.

10uF+0.1uF+0.01uF at one end of socket in support of 3.3 V pins 2 and 4 (in 2230 modules) or pins 4 and 5 (in 1216 modules).

10uF+0.1uF+0.01uF at the other end of the socket in support of 3.3 V pins 72 and 74 (in 2230 modules) or pins 72 and 73 (in 1216 modules).

9.1.12 Wi-Fi wireless disable and HW RF-KILL

W_DISABLE1# (pin 56 in M.2 2230 pinout, pin 28 in M.2 1216 SD pinout) serves as HW RF-KILL for the Wi-Fi radio. The pin is recommended to be left unconnected if the HW RF-KILL signal is not required.

Asserting W_DISABLE#_1 signal will result in a complete shutdown of the Wi-Fi part.

Table 9-5 W_DISABLE1# characteristics

Characteristic	Description
Internal pull-up resistor	min 100 kOhm, max 200kOhm
VIL for asserting	min 0V, max 0.6V
VIH for de-asserting	min 1.26V, max 3.3V or float (not connected)

9.1.13 M.2 Bluetooth® HW RF-KILL

W_DISABLE2# (pin 54 in M.2 2230 pinout, pin 63 in M.2 1216 SD pinout) serves as HW RF-KILL for the Bluetooth® radio.

Asserting W_DISABLE#_2 signal will result in a complete shutdown of the Bluetooth® part. The result from the user perspective is similar to removing the Bluetooth® device from the platform.

Table 9-6 W_DISABLE2# characteristics

Characteristic	Description
Internal pull-up resistor	min 100 kOhm, max 200kOhm
VIL for asserting	min 0V, max 0.6V
VIH for de-asserting	min 1.26V, max 3.3V or float (not connected)

The recommendation for using HW RF-KILL functionality is to use a GPIO pin, provided by the ACPI, to turn on/off the radio of the Bluetooth® device. BIOS shall implement ACPI function for HW RF-KILL implementation in the OS. For more information, please refer to Intel document number 559910, "Intel Connectivity Platform BIOS Guidelines," Section 3.1.5.6, "Bluetooth® RTD3 control."



9.1.14 BIOS

The CNVi modules (including Jefferson Peak) require specific BIOS support. A full description of BIOS support needed for the Cannon Lake and Gemini Lake platforms can be found in the Connectivity BIOS Guide documents.

9.2 Boot sequence

During platform power up the SOC/PCH performs a hardware auto-detect handshake to detect the presence of a CRF in the system. From SOC/PCH perspective there can be a CRF in the system, or there can be no CRF, in which case Wi-Fi and Bluetooth® are supported by a discrete connectivity module.

The following signals are involved in the CNVi auto detect sequence:

- CRF power supply – 3.3V power pin of the connectivity module (either CRF or discrete)
- RSMRST# – Platform global resume reset signal
- CNV_RF_RESET# – GPIO used as a reset for CRF modules (output from PCH)
- CNV_RGI_DT – GPIO used as a strap to detect the CRF present and as a control bus for CNVi (PCH strap and output from PCH)
- MODEM_CLKREQ – GPIO used to activate/deactivate the CRF reference clock (output of PCH)
- 38.4Mhz clock – The CRF reference clock (input to PCH)

The auto-detect is based on the CNV_RGI_DT signal which is initially controlled by the CRF and sampled as a PCH strap during power up.

Inside the CRF chip, the CNV_RGI_DT is actively pulled low (with an approximate strength of 1K ohm to ground). This pull-down is only valid when the CRF power is up and stable therefore it is required that the 3.3V power to the connectivity module will ramp up before any auto-detect sequence starts.

The PCH straps are sampled immediately after the de-assertion of RSMRSET#.

- 1) If the system has a CRF, the value sampled into the strap will be the CNV_RGI_DT pulled to zero. In this case once the straps are sampled they are locked and the PCH HW will be configured for CNVi mode until it is shut down.
- 2) Once CNVi HW is configured in the PCH the CNV_RF_RESET# is de-asserted which causes the CRF to de-activate the 1K pull down of CNV_RGI_DT. The CNV_RGI_DT GPIO pin defaults to an output of the PCH to become the RGI bus and is set to logical high (which is the CNV_RGI_DT value at rest).
- 3) As part of the CNVi internal boot, the clock request is asserted by the PCH and the CRF clock starts toggling at a frequency of 38.4Mhz.

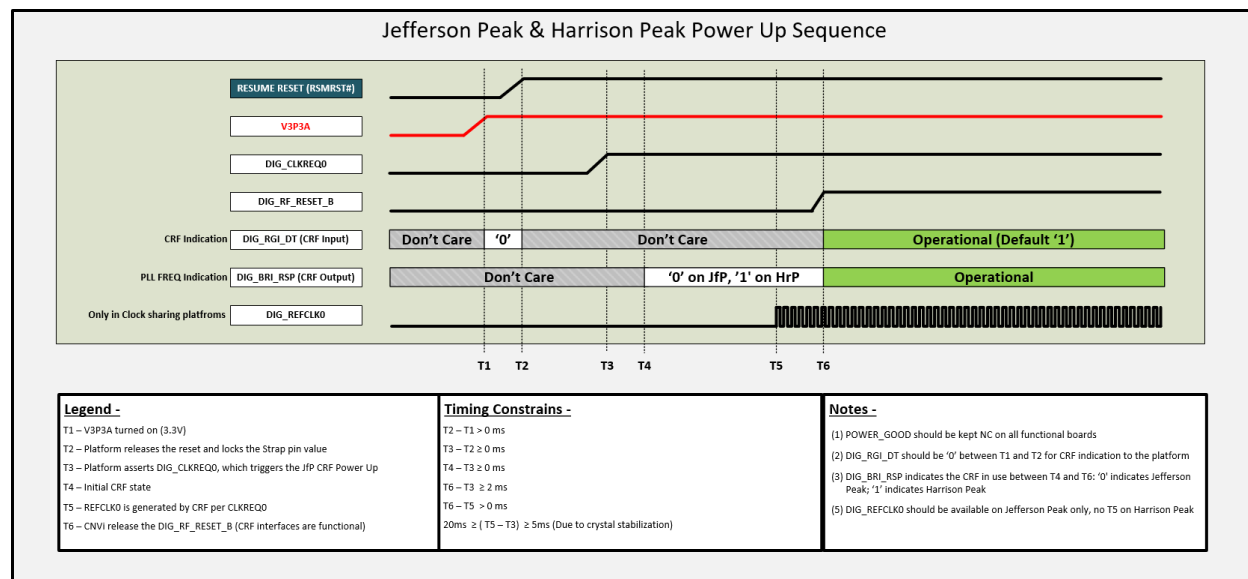
Note: The order between #2 and #3 can change according to the platform.

If, during step (1), the CRF does not exist, the CNV_RGI_DT value will be driven by on-die or platform pull up resistors (typically 20K). In this case, the strap will sample a logical High and the rest of the handshake process will not be performed.



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Figure 9-7 Jefferson Peak power-up sequence





10 GPIO Signals Mapping

Table 10–1 GPIO signals mapping

ICL
CNVI Control

Refer to Section 30.2,
CCL# 574625

PCH-LP

Function	GPIO	BIOS Configuration
CNV_BRI_DT	GPP_F0	Native F1
CNV_BRI_RSP	GPP_F1	Native F1
CNV_RGI_DT	GPP_F2	Native F1
CNV_RGI_RSP	GPP_F3	Native F1
CNV_RF_RESET	GPP_A8* / GPP_F4	Native F2 / F1
MODEM_CLKREQ	GPP_A9* / GPP_F5	Native F2 / F2

* Default

Legacy CNL
CNVI Control

Refer to Section 30.2,
CCL#570374

PCH-LP

Function	GPIO	BIOS Configuration
CNV_BRI_DT	GPP_F4	Native F1
CNV_BRI_RSP	GPP_F5	Native F1
CNV_RGI_DT	GPP_F6	Native F1
CNV_RGI_RSP	GPP_F7	Native F1
CNV_RF_RESET	GPP_H1	Native F3
MODEM_CLKREQ	GPP_H1	Native F3

Power

GPPH

1.8V

PCH-H

Function	GPIO	BIOS Configuration
CNV_BRI_DT	GPP_J4	Native F1
CNV_BRI_RSP	GPP_J5	Native F1
CNV_RGI_DT	GPP_J6	Native F1
CNV_RGI_RSP	GPP_J7	Native F1
CNV_RF_RESET	GPP_D5	Native F3
MODEM_CLKREQ	GPP_D6	Native F3

Power

GPPD

1.8V



GPIO Signals Mapping

Legacy GML
CNVI Control

Refer to Section 29.2,
CCL# 571119

SoC

Function	GPIO	BIOS Configuration
CNV_BRI_DT	GPIO_191	Native F1
CNV_BRI_RSP	GPIO_192	Native F1
CNV_RGI_DT	GPIO_193	Native F1
CNV_RGI_RSP	GPIO_194	Native F1
CNV_RF_RESET	GPIO_195	Native F1
MODEM_CLKREQ	GPIO_196	Native F1





11 Intel® PROSet/Wireless Software for Bluetooth® Technology v20.0

This section describes the architecture, features and functionality of Intel® PROSet/Wireless Software for Bluetooth® v20.x.x.x for Microsoft Windows 10*.

11.1 Base features

Table 11–1 Intel® PROSet/Wireless v20.x.x.x Bluetooth® technology key features

Feature name	Description	Comments
UEFI Support	Support for Bluetooth® Low Energy keyboard and mouse in the pre-boot UEFI environment	Starting with Coffee Lake (CFL) and newer platforms
Advanced Bluetooth®-Wi-Fi CoEx	Real time activity indications and flexible messaging channel	

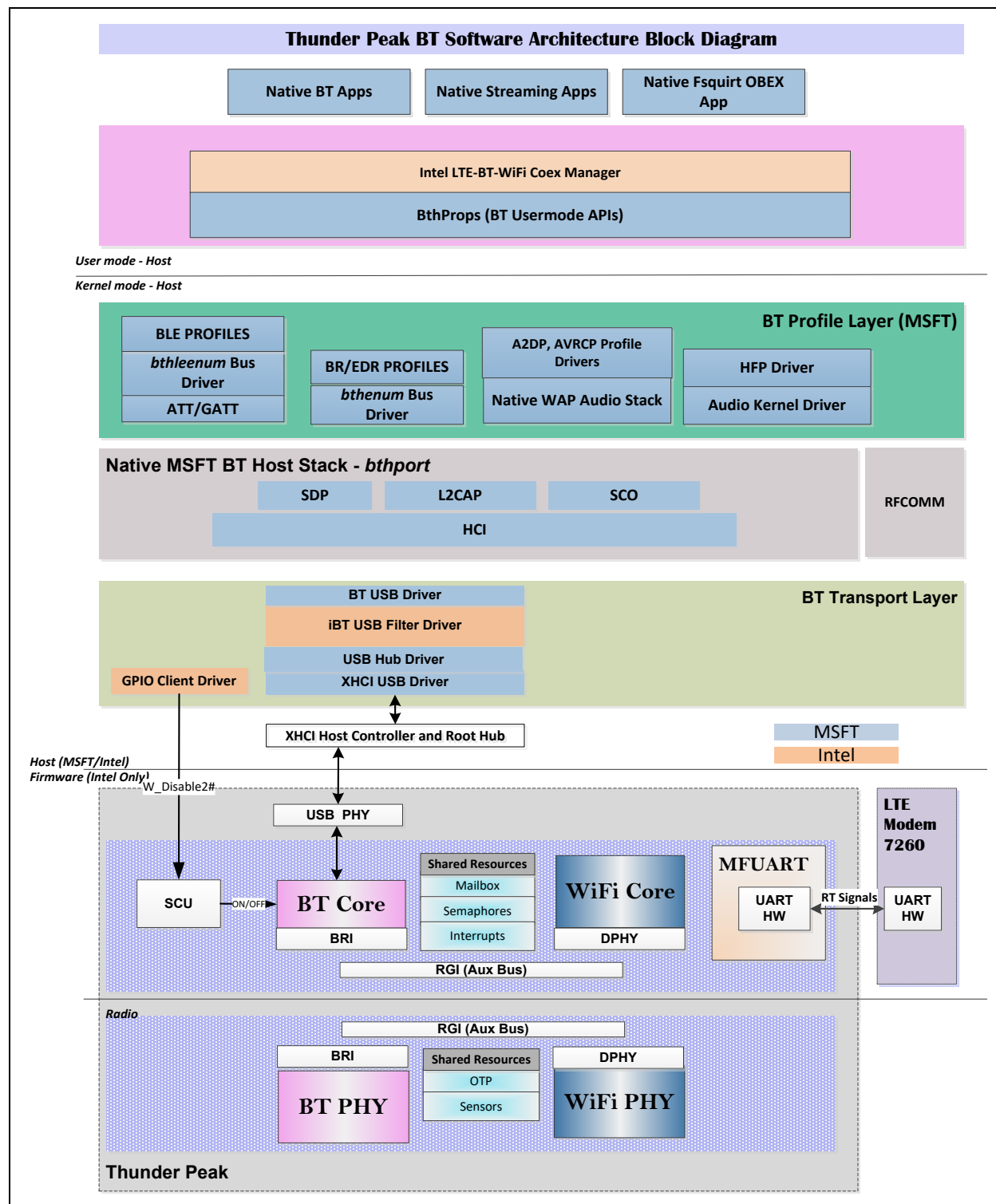
11.2 Bluetooth® software architecture

11.2.1 Bluetooth® host stack

The Bluetooth® Special Interest Group (SIG) specification splits the Bluetooth® protocol between the device (controller) and the host (OS). The Bluetooth® host stack implements the Bluetooth® host part of the protocol. The interface between the Bluetooth® host and the controller is called HCI (Host-Controller Interface), and is also defined by the Bluetooth® SIG.

Figure 11–1 shows the Bluetooth® Stack on Windows 10* for JfP1/JfP2.

Figure 11–1 Jefferson Peak Bluetooth® stack block diagram (Windows 10*)





11.2.1.1 Bluetooth® out-of-box configuration

After installation, the default Bluetooth® controller state in Windows 10 is non-connectable, non-discoverable. There is no RF activity unless commanded by the host. For additional information please see <https://support.microsoft.com/en-us/help/15290/windows-connect-bluetooth-device>.

11.2.1.2 Bluetooth® profiles

The Bluetooth® SIG defines profiles that enable the Bluetooth® use cases and application.

11.2.1.2.1 Supported Bluetooth® profiles

JfP controllers support the native Bluetooth® profiles implemented in Windows 10. For the latest information on Windows 10* Bluetooth® profiles please refer to <https://support.microsoft.com/en-us/help/10568/windows-10-supported-bluetooth-profiles>.

11.2.2 Bluetooth® 4.1 controller features

The Jefferson Peak 1 controller supports the following optional Bluetooth® 4.1 features:

- LE Dual Mode and Link Layer Topology
- BR/EDR Secure Connection
- LE Link Layer Ping
- LE Low Duty Cycle Directed Advertising

LE Dual Mode Topology and Link Layer Topology allow more complex topologies/usage models such as enabling a dual mode ((BR/EDR)LE) device, for example, a smartphone acting as a Bluetooth® Hub (Central) and Bluetooth® peripheral at the same time. A device acting as a Bluetooth® Hub (Central) can be connected to multiple peripherals. A peripheral device can be connected to multiple Hubs (Central).

BR/EDR Secure Connection upgrades Secure Simple Pairing to utilize the P-256 elliptic curve, and device authentication to use FIPS-approved algorithms (HMAC-SHA-256 and AES-CTR). Secure Connections also added message integrity (AES-CCM).

The LE Link Layer Ping procedure can be used at the Link Layer to verify presence of the remote Link Layer. The procedure can also be used to verify message integrity on the LE Asynchronous Control Link (ACL) logical transport by forcing the remote device to send an LE ACL packet that contains a valid Message Integrity Code (MIC).

LE Low Duty Cycle Directed Advertising is designed for cases where reconnection with a specific device is required, but time is not of the essence or it is not known if the central device is in range or not.



11.2.3 Bluetooth® 5 controller optional features

Jefferson Peak 1 modules are Bluetooth® 5 controllers and support the following optional features:

- Slot Availability Mask
- 2 Mbps LE
- LE Long Range
- LE Advertising Extensions
- LE Channel Selection Algorithm #2
- Limited High Duty Cycle Non-connectable Advertising

These optional features need to be supported by Microsoft* before they can be used at a system level. Please consult with Microsoft for information on Windows* support for these features.

The Slot Availability Mask feature, defined by the Bluetooth® SIG, allows a Bluetooth® device to indicate the availability of its slots, for both transmission and reception, to a peer device. This feature improves Bluetooth® device performance in certain scenarios (mainly BR/EDR) such as the LTE Coexistence scenario and Topology management.

The 2 Mbps LE feature enables the Bluetooth® controller to achieve twice the data transfer rate compared to Bluetooth® version 4.2. Benefit: Lower power consumption with faster transfer.

With the LE Long Range feature, Bluetooth® can maintain a connection over a greater distance with e.g. compatible headphones, speakers and fitness trackers.

The LE Advertisement Extensions help with Synchronized Advertisement and Extended Advertisement Packet Length, and provide support for the LE Long Range feature, and Multi-Advertiser Support.

Limited High Duty Cycle Non-Connectable Advertising is a feature where advertising is done using intervals of less than 100ms (down to 20ms) for limited periods of time. Typical applications include advanced beacons and related use cases.

11.2.4 Bluetooth® 5.1 controller features

Jefferson Peak 2 is Bluetooth® 5.1-compliant. The Bluetooth® controller is compliant with Bluetooth® SIG Errata Service Releases ESR11 and ESR12. However, no optional features have been added.

11.3 Bluetooth® product features

11.3.1 Power management

The Bluetooth® Controller supports three power management modes from a software point of view, regardless of the bus the Bluetooth® Controller is connected to. The Windows* Bluetooth® driver owns the definition of and transition in and out of these power management modes.

Table 11-2 Bluetooth® power management

Device Power State (Dx)	Radio Mode	Description	Comments
D0	Active	The Bluetooth® radio is actively communicating with an associated device. This is the highest power state	
D1	Low Power	This state has been deprecated	N/A



Device Power State (Dx)	Radio Mode	Description	Comments
D2	Low Power	The Bluetooth® radio is in a low-power state. The Bluetooth® Controller has been paired with a Bluetooth® device; however, there is no connection between the two – i.e. the device has been disconnected. The Bluetooth® controller must be able to generate a wake signal to the host when new data arrives from the paired device. - or - The Bluetooth® radio has no associations. - or - The Bluetooth® radio has an active connection that is idle (no data being sent/received) and the link is in sniff mode.	This state is equivalent to Selective Suspend.
D3Hot	Low Power	This is the lowest possible low-power state. There is no scanning to support wake in this state, i.e. the device cannot wake the system from this state.	D3Hot is the only device state that can be entered directly from D0.
D3Cold	Off	The Bluetooth® radio is completely off. The Bluetooth® radio is not capable of generating a wake signal to the host in this state. For more detail on power states, please see https://docs.microsoft.com/en-us/windows-hardware/drivers/kernel/device-sleeping-states .	In D3Cold, the device is physically connected to the bus but cannot be detected. D3Cold can only be entered from D3Hot. The transport bus driver or system ACPI firmware may remove power or toggle GPIO lines to transition the Bluetooth radio hardware to the Off mode.

11.3.1.1 USB Selective Suspend

Jefferson Peak 1 supports the USB Selective Suspend power management feature.

11.3.1.2 Modern Standby (MS)

Modern standby is an S0 low-power idle mode. Windows 10* Modern Standby (MS) expands the Windows 8.1* Connected Standby power model to be more inclusive, and allows systems based on rotational media and hybrid media (for example, SSD + HDD or SSHD), and/or a controller that doesn't support all of the prior requirements for Connected Standby to still take advantage of the low power idle model.

HID devices such as keyboards, mice, or other user-input devices will cause the Bluetooth® radio to wake up the platform (e.g. the display will turn on). Not all Bluetooth® devices will wake up the platform (e.g., headphones will not wake up the system).

When in MS and the device is paired it will be in D2 state. Certain events will cause the host to wake up and turn on the display. For more information on waking from MS see <https://docs.microsoft.com/en-us/windows-hardware/design/device-experiences/modern-standby-wake>.



11.3.1.3 Wake On Bluetooth® (WoBT)

Wake on Bluetooth® (WoBT), which is defined as the ability to wake the platform from S3 or S4 via a Bluetooth HID device, is supported by Jefferson Peak 1, but is disabled by default on install. WoBT on JfP1 can be enabled via an extension INF mechanism. Please see your Intel account manager for details.

Note: For this feature to work correctly when the platform is in S3/S4 state, the Bluetooth controller must have power and must not be in RF-Kill, and platform must be capable of detecting USB in-band wake (not in Deep-Sx state) or UART sideband wake (GPIO).

11.3.2 Airplane mode

The Bluetooth radio must support the capability to turn off the radio through the radio management user interface. This user interface control is built into Windows 10. When the Bluetooth® radio has been turned off through this user interface, the radio will be transitioned to the D3 power state and is expected to consume negligible power.

11.3.3 Security

Jefferson Peak 1 supports the BR/EDR Secure Connections feature of the Bluetooth® Core Specification version 4.1, in which device authentication uses FIPS approved algorithms (HMAC-SHA-256) and encryption uses AES-CCM instead of E0 Cipher. It is HW ready for the LE Secure Connections feature of the Bluetooth® Core Specification version 4.2, which may be supported in a future Windows 10* release.

The bulk of the Jefferson Peak 1 Controller Firmware resides in RAM. All code downloaded to RAM by the bootloader is downloaded securely, using an SHA-256 hashing algorithm, 2048-bit keys, and an exponent $e=2^{16}+1$ RSA signing algorithm.

11.3.4 Bluetooth®-Wi-Fi coexistence mechanism

The Wi-Fi- Bluetooth® coexistence mechanism in Jefferson Peak 1 is capable of supporting Tx-Tx, Rx-Rx, Tx-Rx, or Rx-Tx concurrency on two antennas. The Tx-Tx and Rx-Rx concurrency can be done while Wi-Fi is in MIMO mode. The Tx-Rx and Rx-Tx concurrency is enabled or disabled on a packet-by-packet basis, based on antenna isolation, transmit power, and received signal level. In cases where concurrency is not allowed, the packet arbiter will determine, on a packet-by-packet basis, whether Bluetooth or Wi-Fi is allowed to transmit or receive, based on the relative priority of the packets to achieve QoS requirements. QoS can be further optimized by dynamic prioritization of the Bluetooth packets relative to the Wi-Fi. Bluetooth® facilitates better performance in the WiFi-Tx / Bluetooth®-Tx and WiFi-Rx / Bluetooth®-Tx modes by optimizing its own transmit power to allow greater concurrency.

11.3.5 LTE-Coex mechanism

A Bulk Acoustic Wave (BAW) filter is deployed in the front end to reduce the out-of-band LTE interference. The Adaptive Frequency Hopping (AFH) algorithm has been enhanced to consider the co-located LTE. Train nudging and generalized interlace scan are supported in Jefferson Peak 1. Peak to further mitigate the LTE coexistence impact. In addition, a non-real-time coex mechanism can be applied using the Intel Coex manager SW component (which supports specific LTE Modem modules).



11.4 Bluetooth® document references

Table 11-3 Bluetooth® document references

Document name	Location
Bluetooth® Core Spec V5.1	https://www.bluetooth.com/wp-content/uploads/2019/03/1901_Feature_Overview_Brief_FINAL.pdf
Bluetooth® Technology Overview	https://www.bluetooth.com/wp-content/uploads/2019/03/Bluetooth-Overview_Final.pdf
Bluetooth® Low Energy Specifications	Please refer to the Bluetooth® SIG website for the latest on core and profile specifications

